

DDR3L SDRAM

MT41K512M4 – 64 Meg x 4 x 8 banks
MT41K256M8 – 32 Meg x 8 x 8 banks
MT41K128M16 – 16 Meg x 16 x 8 banks

Description

The 1.35V DDR3L SDRAM device is a low-voltage version of the 1.5V DDR3 SDRAM device. Refer to the DDR3 (1.5V) SDRAM data sheet specifications when running in 1.5V compatible mode.

Features

- $V_{DD} = V_{DDQ} = 1.35V$ (1.283–1.45V)
- Backward-compatible to $V_{DD} = V_{DDQ} = 1.5V \pm 0.075V$
- Differential bidirectional data strobe
- 8n-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS (READ) latency (CL)
- Programmable posted CAS additive latency (AL)
- Programmable CAS (WRITE) latency (CWL)
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of 95°C
 - 64ms, 8192-cycle refresh up to 85°C
 - 32ms, 8192-cycle refresh at >85°C to 95°C
- Self refresh temperature (SRT)

- Automatic self refresh (ASR)
- Write leveling
- Multipurpose register
- Output driver calibration

Options

- Configuration
 - 512 Meg x 4
 - 256 Meg x 8
 - 128 Meg x 16
- FBGA package (Pb-free) – x4, x8
 - 78-ball (8mm x 10.5mm x 1.2mm) Rev. K
- FBGA package (Pb-free) – x16
 - 96-ball (8mm x 14mm x 1.2mm) Rev. K
- Timing – cycle time
 - 1.07ns @ CL = 13 (DDR3-1866)
 - 1.25ns @ CL = 11 (DDR3-1600)
 - 1.5ns @ CL = 9 (DDR3-1333)
 - 1.875ns @ CL = 7 (DDR3-1066)
- Operating temperature
 - Commercial ($0^{\circ}C \leq T_C \leq +95^{\circ}C$)
 - Industrial ($-40^{\circ}C \leq T_C \leq +95^{\circ}C$)
- Revision

Marking

512M4
256M8
128M16

DA

JT

-107
-125
-15E
-187E

None
IT
:K

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target t_{RCD} - t_{RP} -CL	t_{RCD} (ns)	t_{RP} (ns)	CL (ns)
-107 ^{1, 2, 3}	1866	13-13-13	13.91	13.91	13.91
-125 ^{1, 2}	1600	11-11-11	13.75	13.75	13.75
-15E ¹	1333	9-9-9	13.5	13.5	13.5
-187E	1066	7-7-7	13.1	13.1	13.1

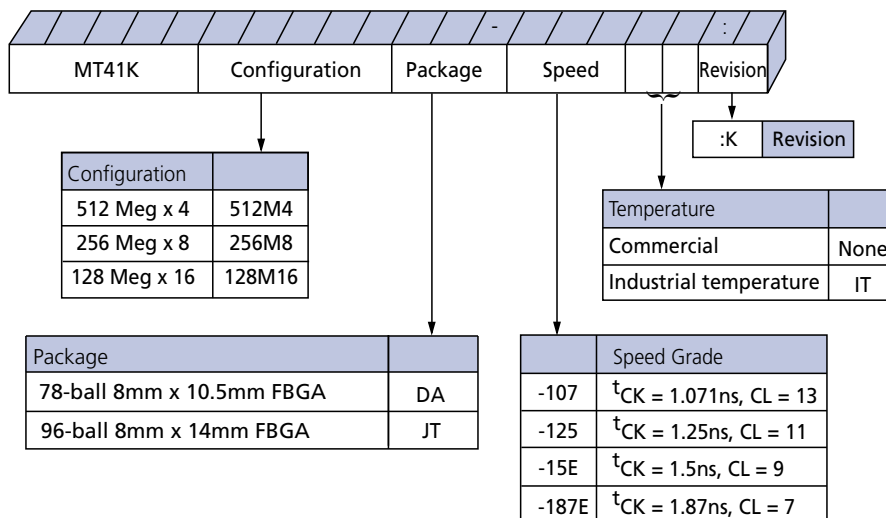
- Notes:
1. Backward compatible to 1066, CL = 7 (-187E).
 2. Backward compatible to 1333, CL = 9 (-15E).
 3. Backward compatible to 1600, CL = 11 (-125).

Table 2: Addressing

Parameter	512 Meg x 4	256 Meg x 8	128 Meg x 16
Configuration	64 Meg x 4 x 8 banks	32 Meg x 8 x 8 banks	16 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row address	32K A[14:0]	32K A[14:0]	16K A[13:0]
Bank address	8 BA[2:0]	8 BA[2:0]	8 BA[2:0]
Column address	2K A[11, 9:0]	1K A[9:0]	1K A[9:0]

Figure 1: DDR3L Part Numbers

Example Part Number: MT41K256M8DA-107:K



Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on <http://www.micron.com> for available offerings.

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: <http://www.micron.com>.

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Important Notes and Warnings

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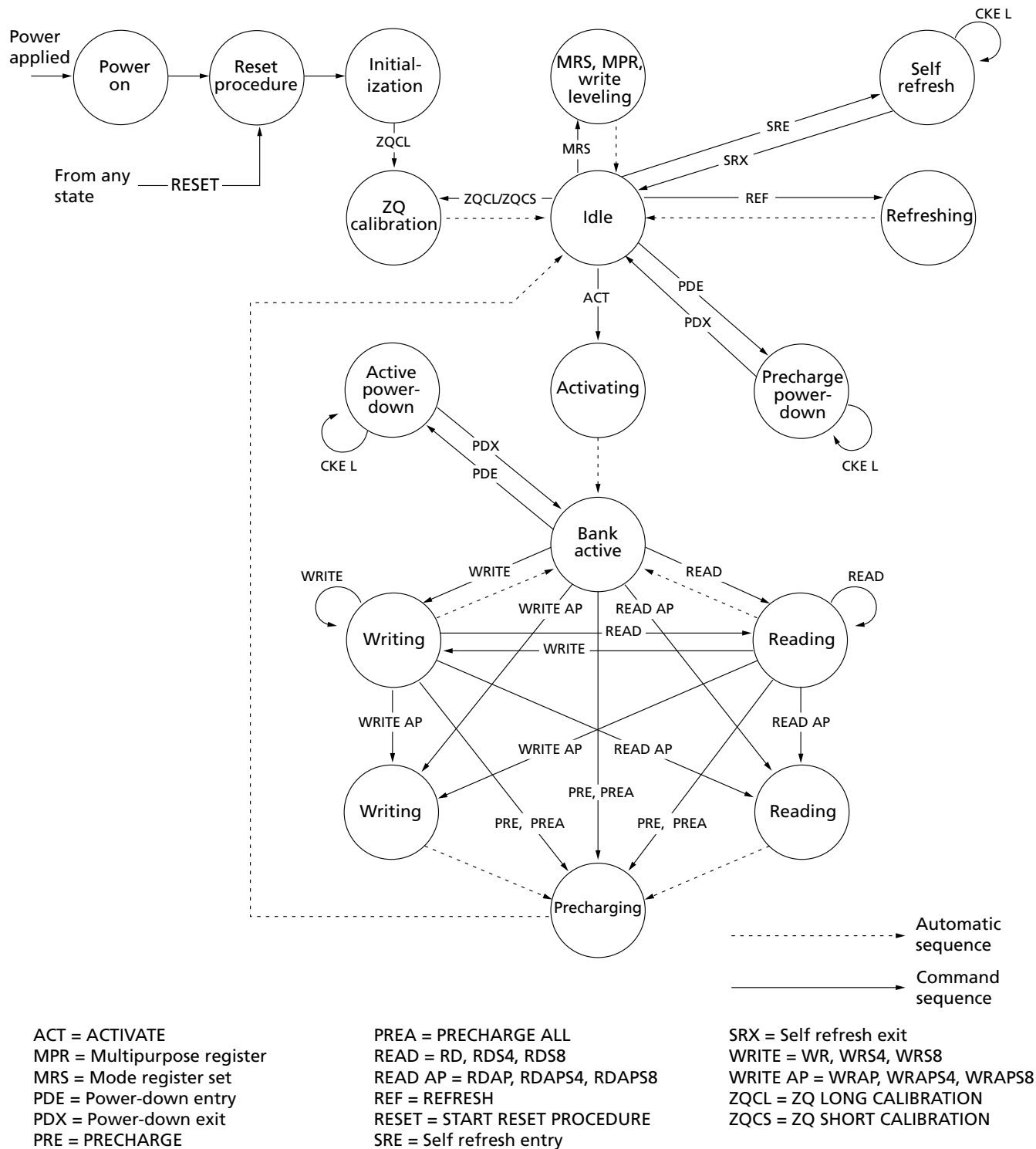
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State Diagram

Figure 2: Simplified State Diagram



Functional Description

DDR3 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an $8n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM effectively consists of a single $8n$ -bit-wide, four-clock-cycle data transfer at the internal DRAM core and eight corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3 SDRAM input receiver. DQS is center-aligned with data for WRITES. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

The DDR3 SDRAM operates from a differential clock (CK and CK#). The crossing of CK going HIGH and CK# going LOW is referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on the first rising edge of DQS after the WRITE preamble, and output data is referenced on the first rising edge of DQS after the READ preamble.

Read and write accesses to the DDR3 SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access.

The device uses a READ and WRITE BL8 and BC4. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

Industrial Temperature

The industrial temperature (IT) device requires that the case temperature not exceed -40°C or 95°C . JEDEC specifications require the refresh rate to double when T_C exceeds 85°C ; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when T_C is $< 0^{\circ}\text{C}$ or $> 95^{\circ}\text{C}$.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation (normal operation).
- Throughout this data sheet, various figures and text refer to DQs as “DQ.” DQ is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
- The terms “DQS” and “CK” found throughout this data sheet are to be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise.

- Complete functionality may be described throughout the document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
 - Any specific requirement takes precedence over a general statement.
 - Any functionality not specifically stated is considered undefined, illegal, and not supported, and can result in unknown operation.
 - Row addressing is denoted as $A[n:0]$. *For example*, 1Gb: $n = 12$ (x16); 1Gb: $n = 13$ (x4, x8); 2Gb: $n = 13$ (x16) and 2Gb: $n = 14$ (x4, x8); 4Gb: $n = 14$ (x16); and 4Gb: $n = 15$ (x4, x8).
 - Dynamic ODT has a special use case: when DDR3 devices are architected for use in a single rank memory array, the ODT ball can be wired HIGH rather than routed. Refer to the Dynamic ODT Special Use Case section.
 - A x16 device's DQ bus is comprised of two bytes. If only one of the bytes needs to be used, use the lower byte for data transfers and terminate the upper byte as noted:
 - Connect UDQS to ground via $1k\Omega^*$ resistor.
 - Connect UDQS# to V_{DD} via $1k\Omega^*$ resistor.
 - Connect UDM to V_{DD} via $1k\Omega^*$ resistor.
 - Connect DQ[15:8] individually to either V_{SS} , V_{DD} , or V_{REF} via $1k\Omega$ resistors, * or float DQ[15:8].
- *If ODT is used, $1k\Omega$ resistor should be changed to 4x that of the selected ODT.

Functional Block Diagrams

DDR3 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 8-bank DRAM.

Figure 3: 512 Meg x 4 Functional Block Diagram

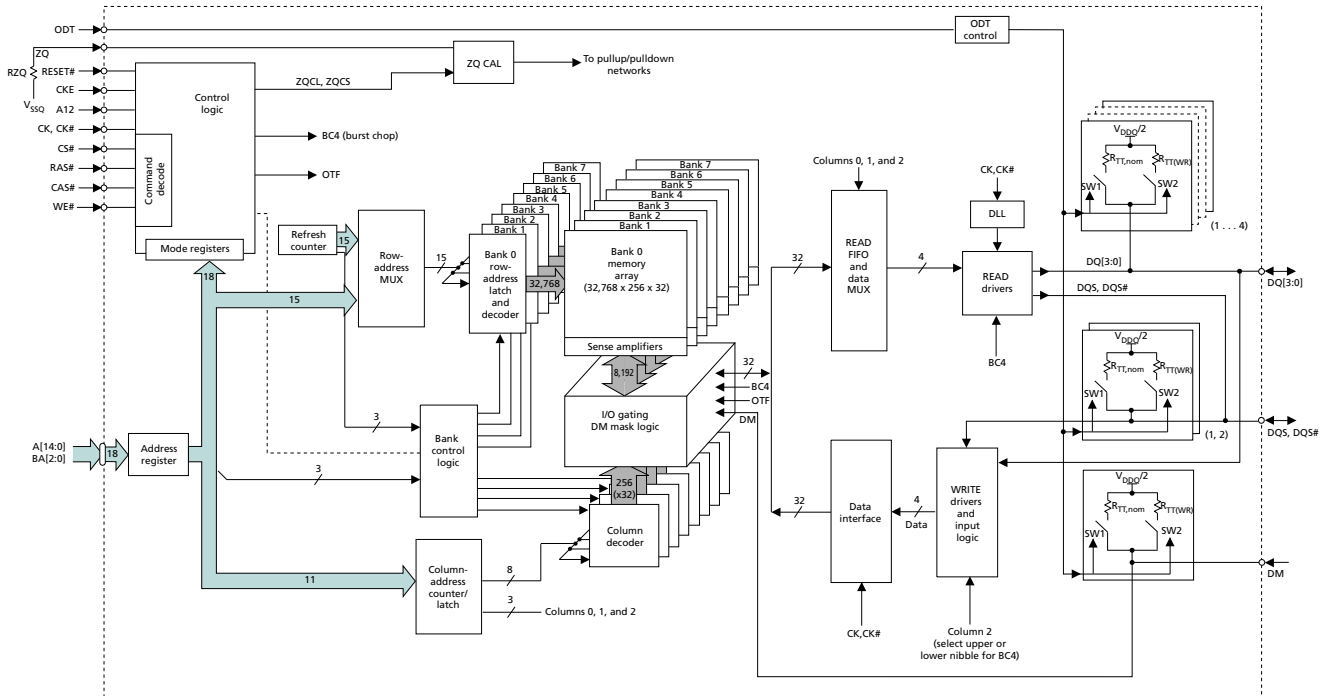


Figure 4: 256 Meg x 8 Functional Block Diagram

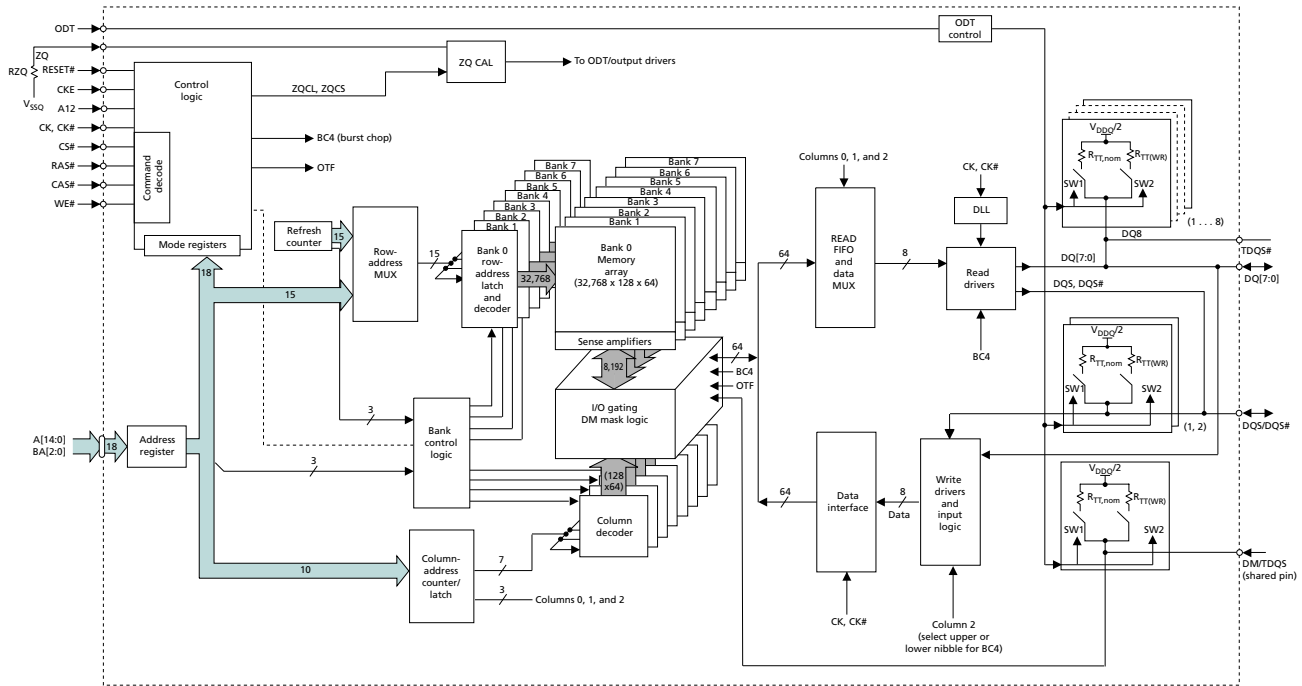
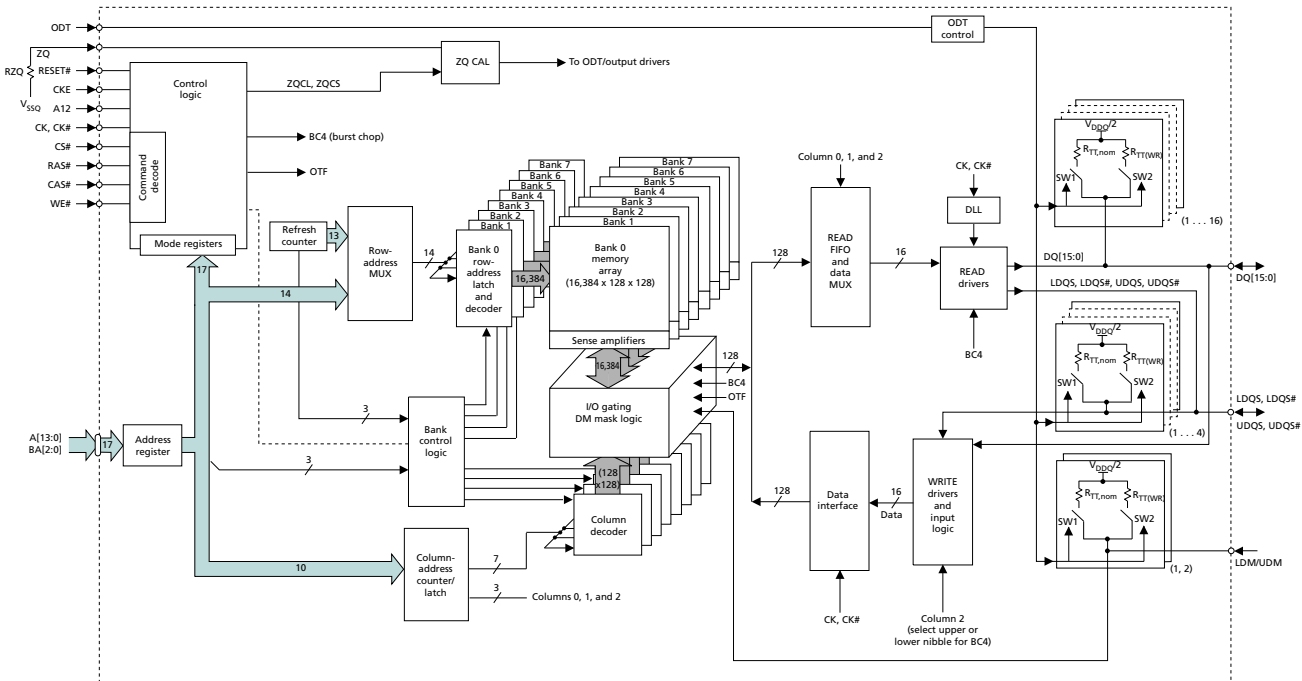


Figure 5: 128 Meg x 16 Functional Block Diagram



Ball Assignments and Descriptions

Figure 6: 78-Ball FBGA – x4, x8 Ball Assignments (Top View)

	1	2	3	4	5	6	7	8	9
A	 V _{SS}	 V _{DD}	 NC				 NF, NF/TDQS#	 V _{SS}	 V _{DD}
B	 V _{SS}	 V _{SSQ}	 DQ0				 DM, DM/TDQS	 V _{SSQ}	 V _{DDQ}
C	 V _{DDQ}	 DQ2	 DQS				 DQ1	 DQ3	 V _{SSQ}
D	 V _{SSQ}	 NF, DQ6	 DQS#				 V _{DD}	 V _{SS}	 V _{SSQ}
E	 V _{REFDQ}	 V _{DDQ}	 NF, DQ4				 NF, DQ7	 NF, DQ5	 V _{DDQ}
F	 NC	 V _{SS}	 RAS#				 CK	 V _{SS}	 NC
G	 ODT	 V _{DD}	 CAS#				 CK#	 V _{DD}	 CKE
H	 NC	 CS#	 WE#				 A10/AP	 ZQ	 NC
J	 V _{SS}	 BA0	 BA2				 NC	 V _{REFCA}	 V _{SS}
K	 V _{DD}	 A3	 A0				 A12/BC#	 BA1	 V _{DD}
L	 V _{SS}	 A5	 A2				 A1	 A4	 V _{SS}
M	 V _{DD}	 A7	 A9				 A11	 A6	 V _{DD}
N	 V _{SS}	 RESET#	 A13				 A14	 A8	 V _{SS}

- Notes:
- Ball descriptions listed in Table 3 (page 20) are listed as “x4, x8” if unique; otherwise, x4 and x8 are the same.
 - A comma separates the configuration; a slash defines a selectable function.
Example: D7 = NF, NF/TDQS#. NF applies to the x4 configuration only. NF/TDQS# applies to the x8 configuration only—selectable between NF or TDQS# via MRS (symbols are defined in Table 3).

Figure 7: 96-Ball FBGA – x16 Ball Assignments (Top View)

	1	2	3	4	5	6	7	8	9
A	 V _{DDQ}	 DQ13	 DQ15				 DQ12	 V _{DDQ}	 V _{SS}
B	 V _{SSQ}	 V _{DD}	 V _{SS}				 UDQS#	 DQ14	 V _{SSQ}
C	 V _{DDQ}	 DQ11	 DQ9				 UDQS	 DQ10	 V _{DDQ}
D	 V _{SSQ}	 V _{DDQ}	 UDM				 DQ8	 V _{SSQ}	 V _{DD}
E	 V _{SS}	 V _{SSQ}	 DQ0				 LDM	 V _{SSQ}	 V _{DDQ}
F	 V _{DDQ}	 DQ2	 LDQS				 DQ1	 DQ3	 V _{SSQ}
G	 V _{SSQ}	 DQ6	 LDQS#				 V _{DD}	 V _{SS}	 V _{SSQ}
H	 V _{REFDQ}	 V _{DDQ}	 DQ4				 DQ7	 DQ5	 V _{DDQ}
J	 NC	 V _{SS}	 RAS#				 CK	 V _{SS}	 NC
K	 ODT	 V _{DD}	 CAS#				 CK#	 V _{DD}	 CKE
L	 NC	 CS#	 WE#				 A10/AP	 ZQ	 NC
M	 V _{SS}	 BA0	 BA2				 NC	 V _{REFCA}	 V _{SS}
N	 V _{DD}	 A3	 A0				 A12/BC#	 BA1	 V _{DD}
P	 V _{SS}	 A5	 A2				 A1	 A4	 V _{SS}
R	 V _{DD}	 A7	 A9				 A11	 A6	 V _{DD}
T	 V _{SS}	 RESET#	 A13				 NC	 A8	 V _{SS}

- Notes:
1. Ball descriptions listed in Table 4 (page 22) are listed as "x16."
 2. A comma separates the configuration; a slash defines a selectable function.

Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions

Symbol	Type	Description
A[14:13], A12/BC#, A11, A10/AP, A[9:0]	Input	Address inputs: Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA} . A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4 burst chop). See Truth Table - Command.
BA[2:0]	Input	Bank address inputs: BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA} .
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	Clock enable: CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle) or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA} .
CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA} .
DM	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to V_{REFDQ} . DM has an optional use as TDQS on the x8 device.
ODT	Input	On-die termination: ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA} .
RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA} .
RESET#	Input	Reset: RESET# is an active LOW CMOS input referenced to V_{SS} . The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH $\geq 0.8 \times V_{\text{DDQ}}$ and DC LOW $\leq 0.2 \times V_{\text{DDQ}}$. RESET# assertion and deassertion are asynchronous.
DQ[3:0]	I/O	Data input/output: Bidirectional data bus for the x4 configuration. DQ[3:0] are referenced to V_{REFDQ} .

Table 3: 78-Ball FBGA – x4, x8 Ball Descriptions (Continued)

Symbol	Type	Description
DQ[7:0]	I/O	Data input/output: Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to V_{REFDQ} .
DQS, DQS#	I/O	Data strobe: Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
TDQS, TDQS#	I/O	Termination data strobe: Applies to the x8 configuration only. When TDQS is enabled, DM is disabled, and the TDQS and TDQS# balls provide termination resistance.
V_{DD}	Supply	Power supply: 1.35V, 1.283–1.45V operational; compatible to 1.5V operation.
V_{DDQ}	Supply	DQ power supply: 1.35V, 1.283–1.45V operational; compatible with 1.5V operation.
V_{REFCA}	Supply	Reference voltage for control, command, and address: V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	Reference voltage for data: V_{REFDQ} must be maintained at all times (including self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	DQ ground: Isolated on the device for improved noise immunity.
ZQ	Reference	External reference ball for output drive calibration: This ball is tied to an external 240Ω resistor (R_{ZQ}), which is tied to V_{SSQ} .
NC	–	No connect: These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).
NF	–	No function: When configured as a x4 device, these balls are NF. When configured as a x8 device, these balls are defined as TDQS#, DQ[7:4].

Table 4: 96-Ball FBGA – x16 Ball Descriptions

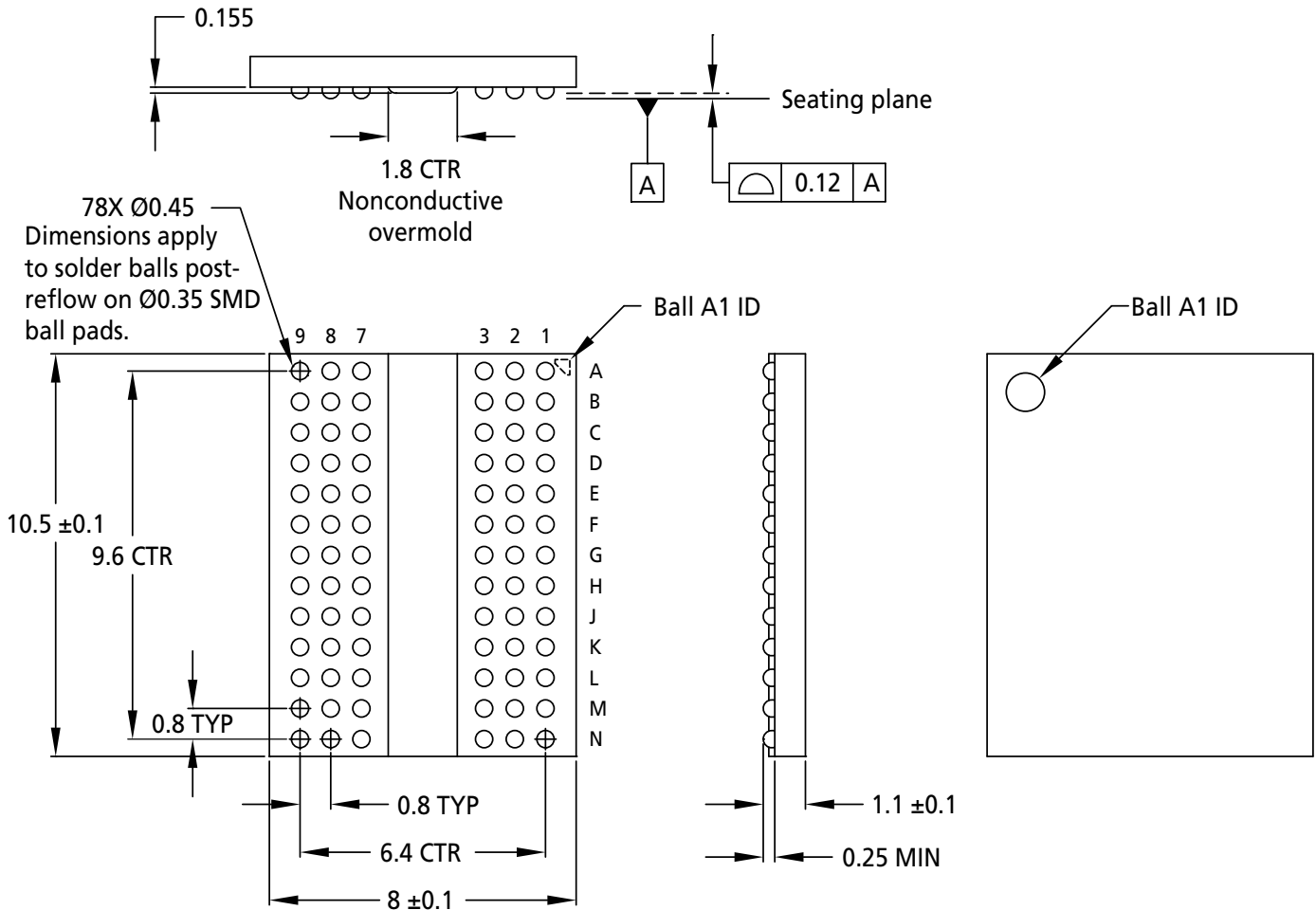
Symbol	Type	Description
A13, A12/BC#, A11, A10/AP, A[9:0]	Input	Address inputs: Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA} . A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4 burst chop). See Truth Table - Command.
BA[2:0]	Input	Bank address inputs: BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA} .
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (LDQS, LDQS#, UDQS, UDQS#) is referenced to the crossings of CK and CK#.
CKE	Input	Clock enable: CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle) or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA} .
CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA} .
LDM	Input	Input data mask: LDM is a lower-byte, input mask signal for write data. Lower-byte input data is masked when LDM is sampled HIGH along with the input data during a write access. Although the LDM ball is input-only, the LDM loading is designed to match that of the DQ and LDQS balls. LDM is referenced to V_{REFDQ} .
ODT	Input	On-die termination: ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[15:0], LDQS, LDQS#, UDQS, UDQS#, LDM, and UDM for the x16. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA} .
RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA} .
RESET#	Input	Reset: RESET# is an active LOW CMOS input referenced to V_{SS} . The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH $\geq 0.8 \times V_{\text{DDQ}}$ and DC LOW $\leq 0.2 \times V_{\text{DDQ}}$. RESET# assertion and deassertion are asynchronous.

Table 4: 96-Ball FBGA – x16 Ball Descriptions (Continued)

Symbol	Type	Description
UDM	Input	Input data mask: UDM is an upper-byte, input mask signal for write data. Upper-byte input data is masked when UDM is sampled HIGH along with the input data during a write access. Although the UDM ball is input-only, the UDM loading is designed to match that of the DQ and UDQS balls. UDM is referenced to V_{REFDQ} .
DQ[7:0]	I/O	Data input/output: Lower byte of bidirectional data bus for the x16 configuration. DQ[7:0] are referenced to V_{REFDQ} .
DQ[15:8]	I/O	Data input/output: Upper byte of bidirectional data bus for the x16 configuration. DQ[15:8] are referenced to V_{REFDQ} .
LDQS, LDQS#	I/O	Lower byte data strobe: Output with read data. Edge-aligned with read data. Input with write data. LDQS is center-aligned to write data.
UDQS, UDQS#	I/O	Upper byte data strobe: Output with read data. Edge-aligned with read data. Input with write data. UDQS is center-aligned to write data.
V_{DD}	Supply	Power supply: 1.35V, 1.283–1.45V operational; compatible to 1.5V operation.
V_{DDQ}	Supply	DQ power supply: 1.35V, 1.283–1.45V operational; compatible with 1.5V operation.
V_{RECA}	Supply	Reference voltage for control, command, and address: V_{RECA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	Reference voltage for data: V_{REFDQ} must be maintained at all times (including self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	DQ ground: Isolated on the device for improved noise immunity.
ZQ	Reference	External reference ball for output drive calibration: This ball is tied to an external 240Ω resistor (R_{ZQ}), which is tied to V_{SSQ} .
NC	–	No connect: These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).

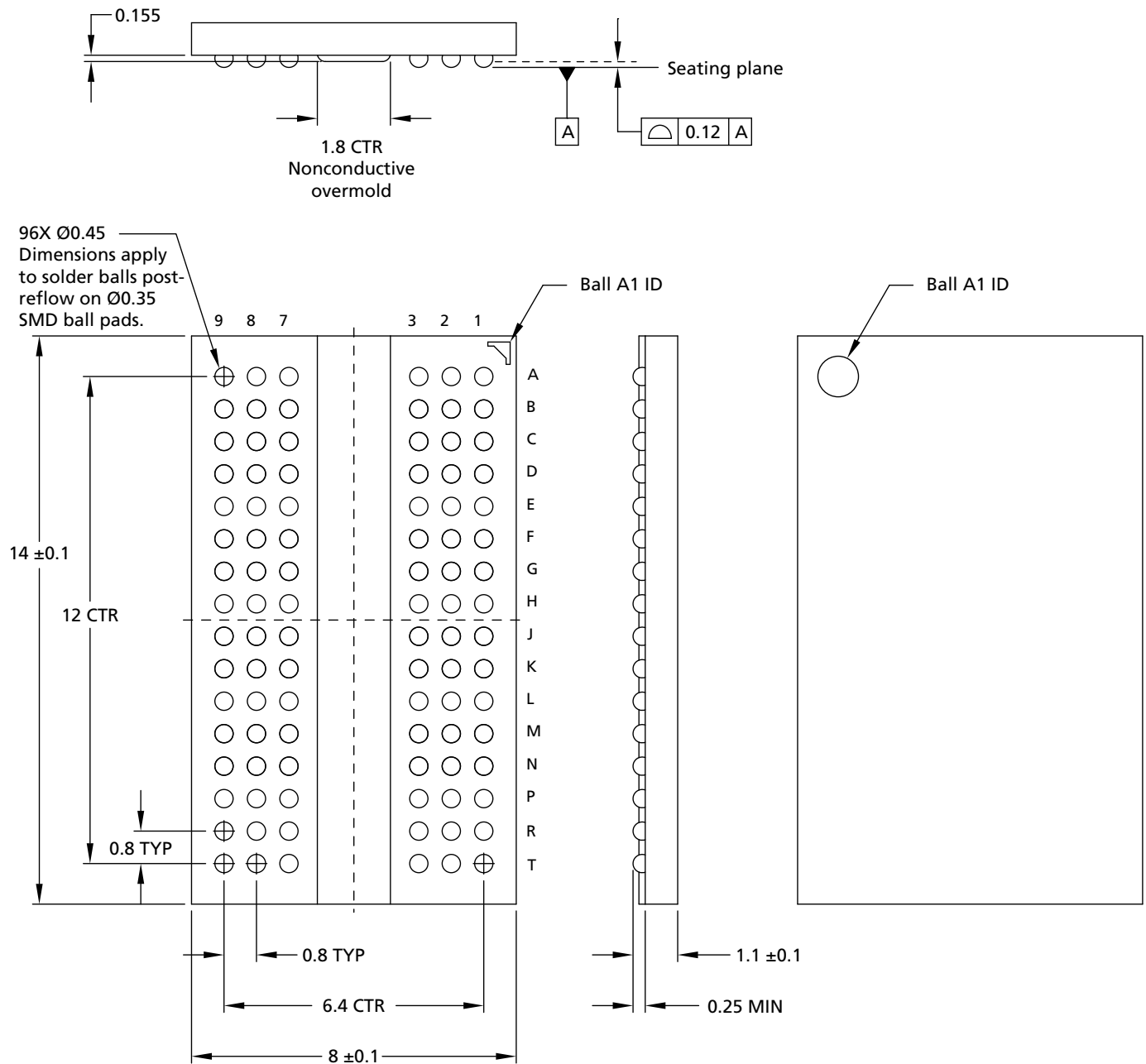
Package Dimensions

Figure 8: 78-Ball FBGA – x4, x8 (DA)



- Notes:
1. All dimensions are in millimeters.
 2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Figure 9: 96-Ball FBGA – x16 (JT)



- Notes:
1. All dimensions are in millimeters.
 2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Electrical Specifications

Table 5: Input/Output Capacitance

Capacitance Parameters	Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single-end I/O: DQ, DM	C_{IO}	1.5	2.5	1.5	2.5	1.5	2.3	1.5	2.2	1.5	2.1	pF
Differential I/O: DQS, DQS#, TDQS, TDQS#	C_{IO}	1.5	2.5	1.5	2.5	1.5	2.3	1.5	2.2	1.5	2.1	pF
Inputs (CTRL, CMD, ADDR)	C_I	0.75	1.3	0.75	1.3	0.75	1.3	0.75	1.2	0.75	1.2	pF

Table 6: DC Electrical Characteristics and Operating Conditions – 1.35V Operation

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
Supply voltage	V_{DD}	1.283	1.35	1.45	V	1, 2, 3, 4
I/O supply voltage	V_{DDQ}	1.283	1.35	1.45	V	1, 2, 3, 4

- Notes:
1. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of $V_{DD}/V_{DDQ}(t)$ over a very long period of time (for example, 1 sec).
 2. If the maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
 3. Under these supply voltages, the device operates to this DDR3L specification.
 4. Once initialized for DDR3L operation, DDR3 operation may only be used if the device is in reset while V_{DD} and V_{DDQ} are changed for DDR3 operation (see Figure 47 (page 141)).

Table 7: DC Electrical Characteristics and Operating Conditions – 1.5V Operation

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Units	Notes
Supply voltage	V_{DD}	1.425	1.5	1.575	V	1, 2, 3
I/O supply voltage	V_{DDQ}	1.425	1.5	1.575	V	1, 2, 3

- Notes:
1. If the minimum limit is exceeded, input levels shall be governed by DDR3L specifications.
 2. Under 1.5V operation, this DDR3L device operates in accordance with the DDR3 specifications under the same speed timings as defined for this device.
 3. Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while V_{DD} and V_{DDQ} are changed for DDR3L operation (see Figure 47 (page 141)).

Table 8: Input Switching Conditions – Command and Address

Parameter/Condition	Symbol	DDR3L-800/1066	DDR3L-1333/1600	DDR3L-1866	Units
Input high AC voltage: Logic 1	$V_{IH(AC160)min}^1$	160	160	–	mV
Input high AC voltage: Logic 1	$V_{IH(AC135)min}^1$	135	135	135	mV
Input high AC voltage: Logic 1	$V_{IH(AC125)min}^1$	–	–	125	mV
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	90	90	mV
Input low DC voltage: Logic 0	$V_{IL(DC90)min}$	–90	–90	–90	mV
Input low AC voltage: Logic 0	$V_{IL(AC125)min}^1$	–	–	–125	mV
Input low AC voltage: Logic 0	$V_{IL(AC135)min}^1$	–135	–135	–135	mV
Input low AC voltage: Logic 0	$V_{IL(AC160)min}^1$	–160	–160	–	mV

Note: 1. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

For example, for DDR3L-800, two input AC levels are defined: $V_{IH(AC160),min}$ and $V_{IH(AC135),min}$ (corresponding $V_{IL(AC160),min}$ and $V_{IL(AC135),min}$). For DDRL-800, the address/command inputs must use either $V_{IH(AC160),min}$ with $t_{IS(AC160)}$ of 215ps or $V_{IH(AC135),min}$ with $t_{IS(AC135)}$ of 365ps; independently, the data inputs may use either $V_{IH(AC160),min}$ or $V_{IH(AC135),min}$.

Table 9: Input Switching Conditions – DQ and DM

Parameter/Condition	Symbol	DDR3L-800/1066	DDR3L-1333/1600	DDR3L-1866	Units
Input high AC voltage: Logic 1	$V_{IH(AC160)min}^1$	160	160	–	mV
Input high AC voltage: Logic 1	$V_{IH(AC135)min}^1$	135	135	135	mV
Input high AC voltage: Logic 1	$V_{IH(AC130)min}^1$	–	–	130	mV
Input high DC voltage: Logic 1	$V_{IH(DC90)min}$	90	90	90	mV
Input low DC voltage: Logic 0	$V_{IL(DC90)min}$	–90	–90	–90	mV
Input low AC voltage: Logic 0	$V_{IL(AC130)min}^1$	–	–	–130	mV
Input low AC voltage: Logic 0	$V_{IL(AC135)min}^1$	–135	–135	–135	mV
Input low AC voltage: Logic 0	$V_{IL(AC160)min}^1$	–160	–160	–	mV

Note: 1. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

For example, for DDR3L-800, two input AC levels are defined: $V_{IH(AC160),min}$ and $V_{IH(AC135),min}$ (corresponding $V_{IL(AC160),min}$ and $V_{IL(AC135),min}$). For DDRL-800, the data inputs must use either $V_{IH(AC160),min}$ with $t_{IS(AC160)}$ of 90ps or $V_{IH(AC135),min}$ with $t_{IS(AC135)}$ of 140ps; independently, the address/command inputs may use either $V_{IH(AC160),min}$ or $V_{IH(AC135),min}$.

Table 10: Differential Input Operating Conditions (CK, CK# and DQS, DQS#)

Parameter/Condition	Symbol	Min	Max	Units
Differential input logic high – slew	$V_{IH,diff(AC)slew}$	180	N/A	mV
Differential input logic low – slew	$V_{IL,diff(AC)slew}$	N/A	-180	mV
Differential input logic high	$V_{IH,diff(AC)}$	$2 \times (V_{IH(AC)} - V_{REF})$	V_{DD}/V_{DDQ}	mV
Differential input logic low	$V_{IL,diff(AC)}$	V_{SS}/V_{SSQ}	$2 \times (V_{IL(AC)} - V_{REF})$	mV
Single-ended high level for strobes	V_{SEH}	$V_{DDQ}/2 + 160$	V_{DDQ}	mV
Single-ended high level for CK, CK#		$V_{DD}/2 + 160$	V_{DD}	mV
Single-ended low level for strobes	V_{SEL}	V_{SSQ}	$V_{DDQ}/2 - 160$	mV
Single-ended low level for CK, CK#		V_{SS}	$V_{DD}/2 - 160$	mV

Table 11: Minimum Required Time t_{DVAC} for CK/CK#, DQS/DQS# Differential for AC Ringback

Slew Rate (V/ns)	DDR3L-800/1066/1333/1600		DDR3L-1866		
	t_{DVAC} at 320mV (ps)	t_{DVAC} at 270mV (ps)	t_{DVAC} at 270mV (ps)	t_{DVAC} at 250mV (ps)	t_{DVAC} at 260mV (ps)
>4.0	189	201	163	168	176
4.0	189	201	163	168	176
3.0	162	179	140	147	154
2.0	109	134	95	105	111
1.8	91	119	80	91	97
1.6	69	100	62	74	78
1.4	40	76	37	52	55
1.2	Note1	44	5	22	24
1.0	Note1	Note1	Note1	Note1	Note1
<1.0	Note1	Note1	Note1	Note1	Note1

Note: 1. Rising input signal shall become equal to or greater than $V_{IH(ac)}$ level and Falling input signal shall become equal to or less than $V_{IL(ac)}$ level.

Table 12: R_{TT} Effective Impedance

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

MR1 [9, 6, 2]	R _{TT}	Resistor	V _{OUT}	Min	Nom	Max	Units
0, 1, 0	120Ω	R _{TT,120PD240}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/1
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/1
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/1
		R _{TT,120PU240}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/1
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/1
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/1
	120Ω		V _{IL(AC)} to V _{IH(AC)}	0.9	1.0	1.65	RZQ/2
0, 0, 1	60Ω	R _{TT,60PD120}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/2
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/2
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/2
		R _{TT,60PU120}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/2
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/2
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/2
	60Ω		V _{IL(AC)} to V _{IH(AC)}	0.9	1.0	1.65	RZQ/4
0, 1, 1	40Ω	R _{TT,40PD80}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/3
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/3
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/3
		R _{TT,40PU80}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/3
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/3
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/3
	40Ω		V _{IL(AC)} to V _{IH(AC)}	0.9	1.0	1.65	RZQ/6
1, 0, 1	30Ω	R _{TT,30PD60}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/4
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/4
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/4
		R _{TT,30PU60}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/4
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/4
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/4
	30Ω		V _{IL(AC)} to V _{IH(AC)}	0.9	1.0	1.65	RZQ/8
1, 0, 0	20Ω	R _{TT,20PD40}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/6
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/6
		R _{TT,20PU40}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/6
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/6
	20Ω		V _{IL(AC)} to V _{IH(AC)}	0.9	1.0	1.65	RZQ/12

Table 13: Reference Settings for ODT Timing Measurements

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

Measured Parameter	$R_{TT,nom}$ Setting	$R_{TT(WR)}$ Setting	V_{SW1}	V_{SW2}
t_{AON}	RZQ/4 (60 Ω)	N/A	50mV	100mv
	RZQ/12 (20 Ω)	N/A	100mV	200mV
t_{AOF}	RZQ/4 (60 Ω)	N/A	50mV	100mv
	RZQ/12 (20 Ω)	N/A	100mV	200mV
t_{AONPD}	RZQ/4 (60 Ω)	N/A	50mV	100mv
	RZQ/12 (20 Ω)	N/A	100mV	200mV
t_{AOFPD}	RZQ/4 (60 Ω)	N/A	50mV	100mv
	RZQ/12 (20 Ω)	N/A	100mV	200mV
t_{ADC}	RZQ/12 (20 Ω)	RZQ/2 (20 Ω)	200mV	250mV

Table 14: 34 Ω Driver Impedance Characteristics

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

MR1 [5, 1]	R _{ON}	Resistor	V _{OUT}	Min	Nom	Max ¹	Units
0, 1	34.3Ω	R _{ON,34PD}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/7
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/7
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/7
		R _{ON,34PU}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/7
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/7
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/7
Pull-up/pull-down mismatch (MM _{PUPD})		V _{IL(AC)} to V _{IH(AC)}	−10	N/A	10	%	

Note: 1. A larger maximum limit will result in slightly lower minimum currents.

Table 15: 40 Ω Driver Impedance Characteristics

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

MR1 [5, 1]	R _{ON}	Resistor	V _{OUT}	Min	Nom	Max ¹	Units
0, 0	40Ω	R _{ON,40PD}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/6
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/6
		R _{ON,40PU}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/6
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/6
Pull-up/pull-down mismatch (MM _{PUPD})		V _{IL(AC)} to V _{IH(AC)}	−10	N/A	10	%	

Note: 1. A larger maximum limit will result in slightly lower minimum currents.

Table 16: Single-Ended Output Driver Characteristics

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

Parameter/Condition	Symbol	Min	Max	Units
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{REF} - 0.09 \times V_{DDQ}$ and $V_{OH(AC)} = V_{REF} + 0.09 \times V_{DDQ}$	SRQ_{se}	1.75	6	V/ns

Table 17: Differential Output Driver Characteristics

Gray-shaded cells have the same values as those in the 1.5V DDR3 data sheet

Parameter/Condition	Symbol	Min	Max	Units
Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)} = -0.18 \times V_{DDQ}$ and $V_{OH,diff(AC)} = 0.18 \times V_{DDQ}$	SRQ_{diff}	3.5	12	V/ns
Output differential crosspoint voltage	$V_{OX(AC)}$	$V_{REF} - 135$	$V_{REF} + 135$	mV

Table 18: Electrical Characteristics and AC Operating Conditions

Note 1 applies to base timing specifications

Parameter		Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
DQ Input Timing													
Data setup time to DQS, DQS#	Base (specification)	$t_{DS}^{(AC160)}$	90	–	40	–	N/A	–	N/A	–	N/A	–	ps
	V_{REF} @ 1 V/ns		250	–	200	–	N/A	–	N/A	–	N/A	–	ps
Data setup time to DQS, DQS#	Base (specification)	$t_{DS}^{(AC135)}$	140	–	90	–	45	–	25	–	N/A	–	ps
	V_{REF} @ 1 V/ns		275	–	225	–	180	–	160	–	N/A	–	ps
Data hold time from DQS, DQS#	Base (specification)	$t_{DH}^{(DC90)}$	160	–	110	–	75	–	55	–	N/A	–	ps
	V_{REF} @ 1 V/ns		250	–	200	–	165	–	145	–	N/A	–	ps
Data setup time to DQS, DQS#	Base (specification)	$t_{DS}^{(AC130)}$	N/A	–	N/A	–	N/A	–	N/A	–	70	–	ps
	V_{REF} @ 2 V/ns		N/A	–	N/A	–	N/A	–	N/A	–	135	–	ps
Data hold time from DQS, DQS#	Base (specification)	$t_{DH}^{(DC90)}$	N/A	–	N/A	–	N/A	–	N/A	–	75	–	ps
	V_{REF} @ 2 V/ns		N/A	–	N/A	–	N/A	–	N/A	–	110	–	ps
Command and Address Timing													
CTRL, CMD, ADDR setup to CK, CK#	Base (specification)	$t_{IS}^{(AC160)}$	215	–	140	–	80	–	60	–	N/A	–	ps
	V_{REF} @ 1 V/ns		375	–	300	–	240	–	220	–	N/A	–	ps

Table 18: Electrical Characteristics and AC Operating Conditions (Continued)

Note 1 applies to base timing specifications

Parameter		Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
CTRL, CMD, ADDR setup to CK, CK#	Base (specification)	t_{IS} (AC135)	365	–	290	–	205	–	185	–	65	–	ps
	V_{REF} @ 1 V/ns		500	–	425	–	340	–	320	–	200	–	ps
CTRL, CMD, ADDR setup to CK, CK#	Base (specification)	t_{IS} (AC125)	N/A	–	N/A	–	N/A	–	N/A	–	150	–	ps
	V_{REF} @ 1 V/ns		N/A	–	N/A	–	N/A	–	N/A	–	275	–	ps
CTRL, CMD, ADDR hold from CK, CK#	Base (specification)	t_{IH} (DC90)	285	–	210	–	150	–	130	–	110	–	ps
	V_{REF} @ 1 V/ns		375	–	300	–	240	–	220	–	200	–	ps

- Notes: 1. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

For example, for DDR3-800, two input AC levels are defined: $V_{IH(AC160),min}$ and $V_{IH(AC135),min}$ (corresponding $V_{IL(AC160),min}$ and $V_{IL(AC135),min}$). For DDR3-800, the address/command inputs must use either $V_{IH(AC160),min}$ with $t_{IS(AC160)}$ of 215ps or $V_{IH(AC135),min}$ with $t_{IS(AC135)}$ of 365ps; independently, the data inputs must use either $V_{IH(AC160),min}$ with $t_{DS(AC160)}$ of 90ps or $V_{IH(AC135),min}$ with $t_{DS(AC135)}$ of 140ps.

2. When DQ single-ended slew rate is 1V/ns, the DQS differential slew rate is 2V/ns; when DQ single-ended slew rate is 2V/ns, the DQS differential slew rate is 4V/ns;

Table 19: Derating Values for t_{IS}/t_{IH} – AC160/DC90-Based

$\Delta t_{IS}, \Delta t_{IH}$ Derating (ps) – AC/DC-Based																
CMD/ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
2.0	80	45	80	45	80	45	88	53	96	61	104	69	112	79	120	95
1.5	53	30	53	30	53	30	61	38	69	46	77	54	85	64	93	80
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	–1	–3	–1	–3	–1	–3	7	5	15	13	23	21	31	31	39	47
0.8	–3	–8	–3	–8	–3	–8	5	1	13	9	21	17	29	27	37	43
0.7	–5	–13	–5	–13	–5	–13	3	–5	11	3	19	11	27	21	35	37
0.6	–8	–20	–8	–20	–8	–20	0	–12	8	–4	16	4	24	14	32	30
0.5	–20	–30	–20	–30	–20	–30	–12	–22	–4	–14	4	–6	12	4	20	20
0.4	–40	–45	–40	–45	–40	–45	–32	–37	–24	–29	–16	–21	–8	–11	0	5

Table 20: Derating Values for t_{IS}/t_{IH} – AC135/DC90-Based

$\Delta t_{IS}, \Delta t_{IH}$ Derating (ps) – AC/DC-Based																
CMD/ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
2.0	68	45	68	45	68	45	76	53	84	61	92	69	100	79	108	95
1.5	45	30	45	30	45	30	53	38	61	46	69	54	77	64	85	80
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	2	–3	2	–3	2	–3	10	5	18	13	26	21	34	31	42	47
0.8	3	–8	3	–8	3	–8	11	1	19	9	27	17	35	27	43	43
0.7	6	–13	6	–13	6	–13	14	–5	22	3	30	11	38	21	46	37
0.6	9	–20	9	–20	9	–20	17	–12	25	–4	33	4	41	14	49	30
0.5	5	–30	5	–30	5	–30	13	–22	21	–14	29	–6	37	4	45	20
0.4	–3	–45	–3	–45	–3	–45	6	–37	14	–29	22	–21	30	–11	38	5

Table 21: Derating Values for t_{IS}/t_{IH} – AC125/DC90-Based

$\Delta t_{IS}, \Delta t_{IH}$ Derating (ps) – AC/DC-Based																
CMD/ADDR Slew Rate V/ns	CK, CK# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
2.0	63	45	63	45	63	45	71	53	79	61	87	69	95	79	103	95
1.5	42	30	42	30	42	30	50	38	58	46	66	54	74	64	82	80
1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
0.9	3	–3	3	–3	3	–3	11	5	19	13	27	21	35	31	43	47
0.8	6	–8	6	–8	6	–8	14	1	22	9	30	17	38	27	46	43
0.7	10	–13	10	–13	10	–13	18	–5	26	3	34	11	42	21	50	37
0.6	16	–20	16	–20	16	–20	24	–12	32	–4	40	4	48	14	56	30
0.5	15	–30	15	–30	15	–30	23	–22	31	–14	39	–6	47	4	55	20
0.4	13	–45	13	–45	13	–45	21	–37	29	–29	37	–21	45	–11	53	5

Table 22: Minimum Required Time t_{VAC} Above $V_{IH(AC)}$ (Below $V_{IL(AC)}$) for Valid ADD/CMD Transition

Slew Rate (V/ns)	DDR3L-800/1066/1333/1600		DDR3L-1866	
	t_{VAC} at 160mV (ps)	t_{VAC} at 135mV (ps)	t_{VAC} at 135mV (ps)	t_{VAC} at 125mV (ps)
>2.0	200	213	200	205
2.0	200	213	200	205
1.5	173	190	178	184
1.0	120	145	133	143
0.9	102	130	118	129
0.8	80	111	99	111
0.7	51	87	75	89
0.6	13	55	43	59
0.5	Note 1	10	Note 1	18
<0.5	Note 1	10	Note 1	18

Note: 1. Rising input signal shall become equal to or greater than $V_{IH(AC)}$ level and falling input signal shall become equal to or less than $V_{IL(AC)}$ level.

Table 23: Derating Values for t_{DS}/t_{DH} – AC160/DC90-Based

$\Delta t_{DS}, \Delta t_{DH}$ Derating (ps) – AC/DC-Based																
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}
2.0	80	45	80	45	80	45										
1.5	53	30	53	30	53	30	61	38								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			-1	-3	-1	-3	7	5	15	13	23	21				
0.8					-3	-8	5	1	13	9	21	17	29	27		
0.7							-3	-5	11	3	19	11	27	21	35	37
0.6									8	-4	16	4	24	14	32	30
0.5											4	6	12	4	20	20
0.4													-8	-11	0	5

Table 24: Derating Values for t_{DS}/t_{DH} – AC135/DC90-Based

$\Delta t_{DS}, \Delta t_{DH}$ Derating (ps) – AC/DC-Based																
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate															
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}
2.0	68	45	68	45	68	45										
1.5	45	30	45	30	45	30	53	38								
1.0	0	0	0	0	0	0	8	8	16	16						
0.9			2	–3	2	–3	10	5	18	13	26	21				
0.8					3	–8	11	1	19	9	27	17	35	27		
0.7							14	–5	22	3	30	11	38	21	46	37
0.6									25	–4	33	4	41	14	49	30
0.5											39	–6	37	4	45	20
0.4													30	–11	38	5

Table 25: Derating Values for t_{DS}/t_{DH} – AC130/DC100-Based at 2V/ns

Shaded cells indicate slew rate combinations not supported

Δ ^t DS, Δ ^t DH Derating (ps) – AC/DC-Based																									
DQ Slew Rate V/ns	DQS, DQS# Differential Slew Rate																								
	8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		
	Δ ^t DS	Δ ^t DH	Δ ^t DS	Δ ^t DH	Δ ^t DS	Δ ^t DH	Δ ^t DS	Δ ^t DH	Δ ^t DS	Δ ^t DH	Δ ^t DS	Δ ^t DH	Δ ^t DS	Δ ^t DH	Δ ^t DS	Δ ^t DH	Δ ^t DS	Δ ^t DH	Δ ^t DS	Δ ^t DH	Δ ^t DS	Δ ^t DH	Δ ^t DS	Δ ^t DH	
4.0	33	23	33	23	33	23																			
3.5	28	19	28	19	28	19	28	19																	
3.0	22	15	22	15	22	15	22	15	22	15															
2.5			13	9	13	9	13	9	13	9	13	9													
2.0					0	0	0	0	0	0	0	0	0	0											
1.5							-22	-15	-22	-15	-22	-15	-22	-15	-14	-7									
1.0									-65	-45	-65	-45	-65	-45	-57	-37	-49	-29							
0.9											-62	-48	-62	-48	-54	-40	-46	-32	-38	-24					
0.8													-61	-53	-53	-45	-45	-37	-37	-29	-29	-19			
0.7															-49	-50	-41	-42	-33	-34	-25	-24	-17	-8	
0.6																	-37	-49	-29	-41	-21	-31	-13	-15	
0.5																			-31	-51	-23	-41	-15	-25	
0.4																					-28	-56	-20	-40	

Table 26: Minimum Required Time t_{VAC} Above $V_{IH(AC)}$ (Below $V_{IL(AC)}$) for Valid DQ Transition

Slew Rate (V/ns)	t_{VAC} at 160mV (ps)	t_{VAC} at 135mV (ps)	t_{VAC} at 130mV (ps)
>2.0	165	113	95
2.0	165	113	95
1.5	138	90	73
1.0	85	45	30
0.9	67	30	16
0.8	45	11	Note1
0.7	16	Note1	–
0.6	Note1	Note1	–
0.5	Note1	Note1	–
<0.5	Note1	Note1	–

Note: 1. Rising input signal shall become equal to or greater than $V_{IH(AC)}$ level and falling input signal shall become equal to or less than $V_{IL(AC)}$ level.

Thermal Characteristics

Table 27: Thermal Characteristics

Parameter/Condition	Value	Unit	Symbol	Notes
Operating case temperature – Commercial	0 to +85	°C	T_C	1, 2, 3
	0 to +95	°C	T_C	1, 2, 3, 4
Operating case temperature – Industrial	–40 to +85	°C	T_C	1, 2, 3
	–40 to +95	°C	T_C	1, 2, 3, 4

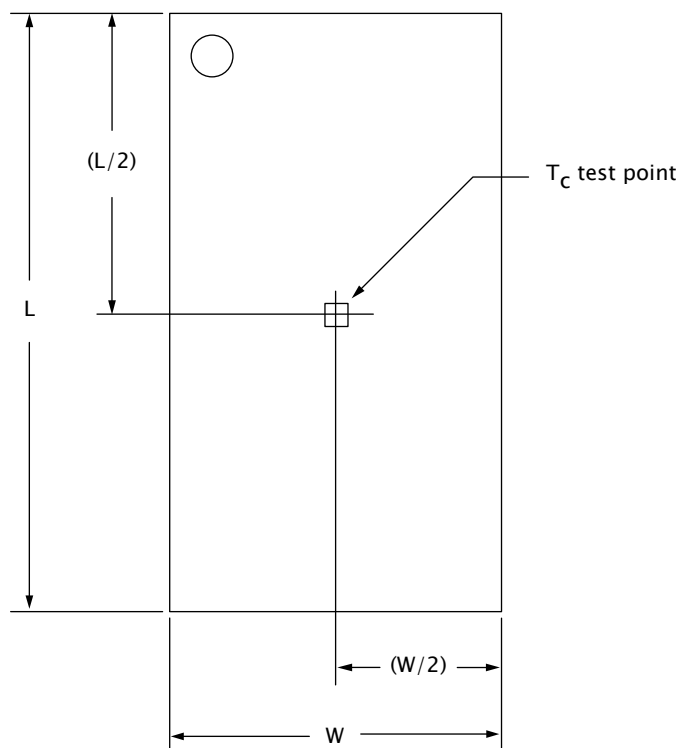
- Notes:
1. Maximum operating case temperature. T_C is measured in the center of the package.
 2. A thermal solution must be designed to ensure the DRAM device does not exceed T_C MAX during operation.
 3. Device functionality is not guaranteed if the DRAM device exceeds T_C MAX during operation.
 4. If T_C exceeds 85°C, the DRAM must be refreshed manually at 2x refresh, which is a 3.9µs interval refresh rate. The use of SRT or ASR must be enabled.
 5. Thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number.

Table 28: Thermal Impedance

Die Rev.	Package	Substrate	Θ_{JA} (°C/W) Airflow = 0m/s	Θ_{JA} (°C/W) Airflow = 1m/s	Θ_{JA} (°C/W) Airflow = 2m/s	Θ_{JB} (°C/W)	Θ_{JC} (°C/W)
K	78-ball	Low conductivity	70.4	56.5	50.8	N/A	6.5
		High conductivity	49.2	42.4	39.3	36.1	N/A
	96-ball	Low conductivity	65.3	52.4	47.1	N/A	6.5
		High conductivity	46.4	40.0	37.2	34.8	N/A

Note: 1. Thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number.

Figure 10: Thermal Measurement Point



Electrical Specifications – I_{DD} Specifications and Conditions

Within the following I_{DD} measurement tables, the following definitions and conditions are used, unless stated otherwise:

- LOW: $V_{IN} \leq V_{IL(AC)max}$; HIGH: $V_{IN} \geq V_{IH(AC)min}$.
- Midlevel: Inputs are $V_{REF} = V_{DD}/2$.
- R_{ON} set to RZQ/7 (34Ω).
- R_{TT,nom} set to RZQ/6 (40Ω).
- R_{TT(WR)} set to RZQ/2 (120Ω).
- Q_{OFF} is enabled in MR1.
- ODT is enabled in MR1 (R_{TT,nom}) and MR2 (R_{TT(WR)}).
- TDQS is disabled in MR1.
- External DQ/DQS/DM load resistor is 25Ω to $V_{DDQ}/2$.
- Burst lengths are BL8 fixed.
- AL equals 0 (except in I_{DD7}).
- I_{DD} specifications are tested after the device is properly initialized.
- Input slew rate is specified by AC parametric test conditions.
- ASR is disabled.
- Read burst type uses nibble sequential (MR0[3] = 0).
- Loop patterns must be executed at least once before current measurements begin.

Table 29: DDR3L Timing Parameters Used for I_{DD} Measurements – Clock Units

I _{DD} Parameter		DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866	Unit
		-25E	-25	-187E	-187	-15E	-15	-125E	-125	-107	
		5-5-5	6-6-6	7-7-7	8-8-8	9-9-9	10-10-10	10-10-10	11-11-11	13-13-13	
t _{CK} (MIN) I _{DD}		2.5		1.875		1.5		1.25		1.07	ns
CL I _{DD}		5	6	7	8	9	10	10	11	13	CK
t _{RCD} (MIN) I _{DD}		5	6	7	8	9	10	10	11	13	CK
t _{RC} (MIN) I _{DD}		20	21	27	28	33	34	38	39	45	CK
t _{RAS} (MIN) I _{DD}		15	15	20	20	24	24	28	28	32	CK
t _{RP} (MIN)		5	6	7	8	9	10	10	11	13	CK
t _{FAW}	x4, x8	16	16	20	20	20	20	24	24	26	CK
	x16	20	20	27	27	30	30	32	32	33	CK
t _{RRD} I _{DD}	x4, x8	4	4	4	4	4	4	5	5	5	CK
	x16	4	4	6	6	5	5	6	6	6	CK
t _{RFC}	1Gb	44	44	59	59	74	74	88	88	103	CK
	2Gb	64	64	86	86	107	107	128	128	150	CK
	4Gb	104	104	139	139	174	174	208	208	243	CK
	8Gb	140	140	187	187	234	234	280	280	328	CK

Table 30: DDR3L I_{DD0} Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
Toggling	Static HIGH	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D	1	0	0	0	0	0	0	0	0	0	0	–
			3	D#	1	1	1	1	0	0	0	0	0	0	0	–
			4	D#	1	1	1	1	0	0	0	0	0	0	0	–
			Repeat cycles 1 through 4 until $nRAS - 1$; truncate if needed													
			$nRAS$	PRE	0	0	1	0	0	0	0	0	0	0	0	–
			Repeat cycles 1 through 4 until $nRC - 1$; truncate if needed													
			nRC	ACT	0	0	1	1	0	0	0	0	0	F	0	–
			$nRC + 1$	D	1	0	0	0	0	0	0	0	0	F	0	–
			$nRC + 2$	D	1	0	0	0	0	0	0	0	0	F	0	–
			$nRC + 3$	D#	1	1	1	1	0	0	0	0	0	F	0	–
			$nRC + 4$	D#	1	1	1	1	0	0	0	0	0	F	0	–
			Repeat cycles $nRC + 1$ through $nRC + 4$ until $nRC - 1 + nRAS - 1$; truncate if needed													
			$nRC + nRAS$	PRE	0	0	1	0	0	0	0	0	0	F	0	–
			Repeat cycles $nRC + 1$ through $nRC + 4$ until $2 \times RC - 1$; truncate if needed													
		1	$2 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 1												
		2	$4 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 2												
		3	$6 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 3												
		4	$8 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 4												
		5	$10 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 5												
		6	$12 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 6												
		7	$14 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 7												

- Notes:
1. DQ, DQS, DQS# are midlevel.
 2. DM is LOW.
 3. Only selected bank (single) active.

Table 31: DDR3L I_{DD1} Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²
Toggling	Static HIGH	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D	1	0	0	0	0	0	0	0	0	0	0	–
			3	D#	1	1	1	1	0	0	0	0	0	0	0	–
			4	D#	1	1	1	1	0	0	0	0	0	0	0	–
			Repeat cycles 1 through 4 until $nRCD - 1$; truncate if needed													
			$nRCD$	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
			Repeat cycles 1 through 4 until $nRAS - 1$; truncate if needed													
			$nRAS$	PRE	0	0	1	0	0	0	0	0	0	0	0	–
			Repeat cycles 1 through 4 until $nRC - 1$; truncate if needed													
			nRC	ACT	0	0	1	1	0	0	0	0	0	F	0	–
			$nRC + 1$	D	1	0	0	0	0	0	0	0	0	F	0	–
			$nRC + 2$	D	1	0	0	0	0	0	0	0	0	F	0	–
			$nRC + 3$	D#	1	1	1	1	0	0	0	0	0	F	0	–
			$nRC + 4$	D#	1	1	1	1	0	0	0	0	0	F	0	–
			Repeat cycles $nRC + 1$ through $nRC + 4$ until $nRC + nRCD - 1$; truncate if needed													
			$nRC + nRCD$	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
			Repeat cycles $nRC + 1$ through $nRC + 4$ until $nRC + nRAS - 1$; truncate if needed													
			$nRC + nRAS$	PRE	0	0	1	0	0	0	0	0	0	F	0	–
			Repeat cycle $nRC + 1$ through $nRC + 4$ until $2 \times nRC - 1$; truncate if needed													
			1	$2 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 1											
			2	$4 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 2											
			3	$6 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 3											
			4	$8 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 4											
			5	$10 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 5											
			6	$12 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 6											
			7	$14 \times nRC$	Repeat sub-loop 0, use BA[2:0] = 7											

- Notes:
1. DQ, DQS, DQS# are midlevel unless driven as required by the RD command.
 2. DM is LOW.
 3. Burst sequence is driven on each DQ signal by the RD command.
 4. Only selected bank (single) active.

Table 32: DDR3L I_{DD} Measurement Conditions for Power-Down Currents

Name	I _{DD2P0} Precharge Power-Down Current (Slow Exit) ¹	I _{DD2P1} Precharge Power-Down Current (Fast Exit) ¹	I _{DD2Q} Precharge Quiet Standby Current	I _{DD3P} Active Power-Down Current
Timing pattern	N/A	N/A	N/A	N/A
CKE	LOW	LOW	HIGH	LOW
External clock	Toggling	Toggling	Toggling	Toggling
t _{CK}	t _{CK} (MIN) I _{DD}	t _{CK} (MIN) I _{DD}	t _{CK} (MIN) I _{DD}	t _{CK} (MIN) I _{DD}
t _{RC}	N/A	N/A	N/A	N/A
t _{RAS}	N/A	N/A	N/A	N/A
t _{RCD}	N/A	N/A	N/A	N/A
t _{RRD}	N/A	N/A	N/A	N/A
t _{RC}	N/A	N/A	N/A	N/A
CL	N/A	N/A	N/A	N/A
AL	N/A	N/A	N/A	N/A
CS#	HIGH	HIGH	HIGH	HIGH
Command inputs	LOW	LOW	LOW	LOW
Row/column addr	LOW	LOW	LOW	LOW
Bank addresses	LOW	LOW	LOW	LOW
DM	LOW	LOW	LOW	LOW
Data I/O	Midlevel	Midlevel	Midlevel	Midlevel
Output buffer DQ, DQS	Enabled	Enabled	Enabled	Enabled
ODT ²	Enabled, off	Enabled, off	Enabled, off	Enabled, off
Burst length	8	8	8	8
Active banks	None	None	None	All
Idle banks	All	All	All	None
Special notes	N/A	N/A	N/A	N/A

- Notes:
1. MR0[12] defines DLL on/off behavior during precharge power-down only; DLL on (fast exit, MR0[12] = 1) and DLL off (slow exit, MR0[12] = 0).
 2. "Enabled, off" means the MR bits are enabled, but the signal is LOW.

Table 33: DDR3L I_{DD2N} and I_{DD3N} Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
Toggling	Static HIGH	0	0	D	1	0	0	0	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D#	1	1	1	1	0	0	0	0	0	F	0	–
			3	D#	1	1	1	1	0	0	0	0	0	F	0	–
		1	4–7	Repeat sub-loop 0, use BA[2:0] = 1												
		2	8–11	Repeat sub-loop 0, use BA[2:0] = 2												
		3	12–15	Repeat sub-loop 0, use BA[2:0] = 3												
		4	16–19	Repeat sub-loop 0, use BA[2:0] = 4												
		5	20–23	Repeat sub-loop 0, use BA[2:0] = 5												
		6	24–27	Repeat sub-loop 0, use BA[2:0] = 6												
		7	28–31	Repeat sub-loop 0, use BA[2:0] = 7												

- Notes: 1. DQ, DQS, DQS# are midlevel.
2. DM is LOW.
3. All banks closed during I_{DD2N}; all banks open during I_{DD3N}.

Table 34: DDR3L I_{DD2NT} Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
Toggling	Static HIGH	0	0	D	1	0	0	0	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D#	1	1	1	1	0	0	0	0	0	F	0	–
			3	D#	1	1	1	1	0	0	0	0	0	F	0	–
		1	4–7	Repeat sub-loop 0, use BA[2:0] = 1; ODT = 0												
		2	8–11	Repeat sub-loop 0, use BA[2:0] = 2; ODT = 1												
		3	12–15	Repeat sub-loop 0, use BA[2:0] = 3; ODT = 1												
		4	16–19	Repeat sub-loop 0, use BA[2:0] = 4; ODT = 0												
		5	20–23	Repeat sub-loop 0, use BA[2:0] = 5; ODT = 0												
		6	24–27	Repeat sub-loop 0, use BA[2:0] = 6; ODT = 1												
		7	28–31	Repeat sub-loop 0, use BA[2:0] = 7; ODT = 1												

- Notes: 1. DQ, DQS, DQS# are midlevel.
2. DM is LOW.
3. All banks closed.

Table 35: DDR3L I_{DD4R} Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ³
Toggling	Static HIGH	0	0	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D#	1	1	1	1	0	0	0	0	0	0	0	–
			3	D#	1	1	1	1	0	0	0	0	0	0	0	–
			4	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	0	0	0	F	0	–
			6	D#	1	1	1	1	0	0	0	0	0	F	0	–
			7	D#	1	1	1	1	0	0	0	0	0	F	0	–
		1	8–15	Repeat sub-loop 0, use BA[2:0] = 1												
		2	16–23	Repeat sub-loop 0, use BA[2:0] = 2												
		3	24–31	Repeat sub-loop 0, use BA[2:0] = 3												
		4	32–39	Repeat sub-loop 0, use BA[2:0] = 4												
		5	40–47	Repeat sub-loop 0, use BA[2:0] = 5												
		6	48–55	Repeat sub-loop 0, use BA[2:0] = 6												
		7	56–63	Repeat sub-loop 0, use BA[2:0] = 7												

- Notes:
1. DQ, DQS, DQS# are midlevel when not driving in burst sequence.
 2. DM is LOW.
 3. Burst sequence is driven on each DQ signal by the RD command.
 4. All banks open.

Table 36: DDR3L I_{DD4W} Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ³
Toggling	Static HIGH	0	0	WR	0	1	0	0	1	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	0	0	0	0	0	–
			2	D#	1	1	1	1	1	0	0	0	0	0	0	–
			3	D#	1	1	1	1	1	0	0	0	0	0	0	–
			4	WR	0	1	0	0	1	0	0	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	0	0	0	F	0	–
			6	D#	1	1	1	1	1	0	0	0	0	F	0	–
			7	D#	1	1	1	1	1	0	0	0	0	F	0	–
		1	8–15	Repeat sub-loop 0, use BA[2:0] = 1												
		2	16–23	Repeat sub-loop 0, use BA[2:0] = 2												
		3	24–31	Repeat sub-loop 0, use BA[2:0] = 3												
		4	32–39	Repeat sub-loop 0, use BA[2:0] = 4												
		5	40–47	Repeat sub-loop 0, use BA[2:0] = 5												
		6	48–55	Repeat sub-loop 0, use BA[2:0] = 6												
		7	56–63	Repeat sub-loop 0, use BA[2:0] = 7												

- Notes:
1. DQ, DQS, DQS# are midlevel when not driving in burst sequence.
 2. DM is LOW.
 3. Burst sequence is driven on each DQ signal by the WR command.
 4. All banks open.

Table 37: DDR3L I_{DD5B} Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data
Toggling	Static HIGH	0	0	REF	0	0	0	1	0	0	0	0	0	0	0	–
		1a	1	D	1	0	0	0	0	0	0	0	0	0	0	–
			2	D	1	0	0	0	0	0	0	0	0	0	0	–
			3	D#	1	1	1	1	0	0	0	0	0	F	0	–
			4	D#	1	1	1	1	0	0	0	0	0	F	0	–
		1b	5–8	Repeat sub-loop 1a, use BA[2:0] = 1												
		1c	9–12	Repeat sub-loop 1a, use BA[2:0] = 2												
		1d	13–16	Repeat sub-loop 1a, use BA[2:0] = 3												
		1e	17–20	Repeat sub-loop 1a, use BA[2:0] = 4												
		1f	21–24	Repeat sub-loop 1a, use BA[2:0] = 5												
		1g	25–28	Repeat sub-loop 1a, use BA[2:0] = 6												
		1h	29–32	Repeat sub-loop 1a, use BA[2:0] = 7												
		2	33–nRFC - 1	Repeat sub-loop 1a through 1h until nRFC - 1; truncate if needed												

Notes: 1. DQ, DQS, DQS# are midlevel.
2. DM is LOW.

Table 38: DDR3L I_{DD} Measurement Conditions for I_{DD6} , I_{DD6ET} , and I_{DD8}

I_{DD} Test	I_{DD6} : Self Refresh Current Normal Temperature Range $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	I_{DD6ET} : Self Refresh Current Extended Temperature Range $T_C = 0^{\circ}\text{C}$ to $+95^{\circ}\text{C}$	I_{DD8} : Reset ²
CKE	LOW	LOW	Midlevel
External clock	Off, CK and CK# = LOW	Off, CK and CK# = LOW	Midlevel
t_{CK}	N/A	N/A	N/A
t_{RC}	N/A	N/A	N/A
t_{RAS}	N/A	N/A	N/A
t_{RCD}	N/A	N/A	N/A
t_{RRD}	N/A	N/A	N/A
t_{RC}	N/A	N/A	N/A
CL	N/A	N/A	N/A
AL	N/A	N/A	N/A
CS#	Midlevel	Midlevel	Midlevel
Command inputs	Midlevel	Midlevel	Midlevel
Row/column addresses	Midlevel	Midlevel	Midlevel
Bank addresses	Midlevel	Midlevel	Midlevel
Data I/O	Midlevel	Midlevel	Midlevel
Output buffer DQ, DQS	Enabled	Enabled	Midlevel
ODT ¹	Enabled, midlevel	Enabled, midlevel	Midlevel
Burst length	N/A	N/A	N/A
Active banks	N/A	N/A	None
Idle banks	N/A	N/A	All
SRT	Disabled (normal)	Enabled (extended)	N/A
ASR	Disabled	Disabled	N/A

- Notes:
1. "Enabled, midlevel" means the MR command is enabled, but the signal is midlevel.
 2. During a cold boot RESET (initialization), current reading is valid after power is stable and RESET has been LOW for 1ms; During a warm boot RESET (while operating), current reading is valid after RESET has been LOW for 200ns + t_{RFC} .

Table 39: DDR3L I_{DD7} Measurement Loop

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ³
Toggling	Static HIGH	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	–
			1	RDA	0	1	0	1	0	0	0	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	0	0	0	0	0	–
			3	Repeat cycle 2 until $nRRD - 1$												
		1	$nRRD$	ACT	0	0	1	1	0	1	0	0	0	F	0	–
			$nRRD + 1$	RDA	0	1	0	1	0	1	0	1	0	F	0	00110011
			$nRRD + 2$	D	1	0	0	0	0	1	0	0	0	F	0	–
			$nRRD + 3$	Repeat cycle $nRRD + 2$ until $2 \times nRRD - 1$												
		2	$2 \times nRRD$	Repeat sub-loop 0, use BA[2:0] = 2												
		3	$3 \times nRRD$	Repeat sub-loop 1, use BA[2:0] = 3												
		4	$4 \times nRRD$	D	1	0	0	0	0	3	0	0	0	F	0	–
			$4 \times nRRD + 1$	Repeat cycle $4 \times nRRD$ until $nFAW - 1$, if needed												
		5	$nFAW$	Repeat sub-loop 0, use BA[2:0] = 4												
		6	$nFAW + nRRD$	Repeat sub-loop 1, use BA[2:0] = 5												
		7	$nFAW + 2 \times nRRD$	Repeat sub-loop 0, use BA[2:0] = 6												
		8	$nFAW + 3 \times nRRD$	Repeat sub-loop 1, use BA[2:0] = 7												
		9	$nFAW + 4 \times nRRD$	D	1	0	0	0	0	7	0	0	0	F	0	–
			$nFAW + 4 \times nRRD + 1$	Repeat cycle $nFAW + 4 \times nRRD$ until $2 \times nFAW - 1$, if needed												
		10	$2 \times nFAW$	ACT	0	0	1	1	0	0	0	0	0	F	0	–
			$2 \times nFAW + 1$	RDA	0	1	0	1	0	0	0	1	0	F	0	00110011
			$2 \times nFAW + 2$	D	1	0	0	0	0	0	0	0	0	F	0	–
			$2 \times nFAW + 3$	Repeat cycle $2 \times nFAW + 2$ until $2 \times nFAW + nRRD - 1$												
		11	$2 \times nFAW + nRRD$	ACT	0	0	1	1	0	1	0	0	0	0	0	–
			$2 \times nFAW + nRRD + 1$	RDA	0	1	0	1	0	1	0	1	0	0	0	00000000
			$2 \times nFAW + nRRD + 2$	D	1	0	0	0	0	1	0	0	0	0	0	–
			$2 \times nFAW + nRRD + 3$	Repeat cycle $2 \times nFAW + nRRD + 2$ until $2 \times nFAW + 2 \times nRRD - 1$												
		12	$2 \times nFAW + 2 \times nRRD$	Repeat sub-loop 10, use BA[2:0] = 2												
		13	$2 \times nFAW + 3 \times nRRD$	Repeat sub-loop 11, use BA[2:0] = 3												
		14	$2 \times nFAW + 4 \times nRRD$	D	1	0	0	0	0	3	0	0	0	0	0	–
			$2 \times nFAW + 4 \times nRRD + 1$	Repeat cycle $2 \times nFAW + 4 \times nRRD$ until $3 \times nFAW - 1$, if needed												
		15	$3 \times nFAW$	Repeat sub-loop 10, use BA[2:0] = 4												

Table 39: DDR3L I_{DD7} Measurement Loop (Continued)

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ³
Toggling	Static HIGH	16	$3 \times nFAW + nRRD$	Repeat sub-loop 11, use BA[2:0] = 5												
		17	$3 \times nFAW + 2 \times nRRD$	Repeat sub-loop 10, use BA[2:0] = 6												
		18	$3 \times nFAW + 3 \times nRRD$	Repeat sub-loop 11, use BA[2:0] = 7												
		19	$3 \times nFAW + 4 \times nRRD$	D	1	0	0	0	0	7	0	0	0	0	0	–
			$3 \times nFAW + 4 \times nRRD + 1$	Repeat cycle $3 \times nFAW + 4 \times nRRD$ until $4 \times nFAW - 1$, if needed												

- Notes:
1. DQ, DQS, DQS# are midlevel unless driven as required by the RD command.
 2. DM is LOW.
 3. Burst sequence is driven on each DQ signal by the RD command.
 4. AL = CL-1.

Electrical Characteristics – I_{DD} Specifications

Table 40: I_{DD} Maximum Limits – Die Rev. K

Speed Bin		DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	Units	Notes
I _{DD}	Width						
I _{DD0}	x4, x8	36	38	39	40	mA	1, 2
	x16	43	45	46	48	mA	1, 2
I _{DD1}	x4	43	47	49	52	mA	1, 2
	x8	46	50	52	54	mA	1, 2
	x16	58	63	65	68	mA	1, 2
I _{DD2P0} (Slow)	All	12	12	12	12	mA	1, 2
I _{DD2P1} (Fast)	All	14	14	14	14	mA	1, 2
I _{DD2Q}	All	20	20	20	20	mA	1, 2
I _{DD2N}	All	21	21	21	21	mA	1, 2
I _{DD2NT}	x4, x8	26	29	31	33	mA	1, 2
	x16	30	33	34	36	mA	1, 2
I _{DD3P}	All	21	21	21	21	mA	1, 2
I _{DD3N}	x4,x8	28	30	32	34	mA	1, 2
	x16	30	33	34	36	mA	1, 2
I _{DD4R}	x4	64	78	90	100	mA	1, 2
	x8	68	82	94	104	mA	1, 2
	x16	88	108	128	148	mA	1, 2
I _{DD4W}	x4	69	81	93	105	mA	1, 2
	x8	73	85	97	108	mA	1, 2
	x16	99	119	138	156	mA	1, 2
I _{DD5B}	All	177	179	180	182	mA	1, 2
I _{DD6}	All	12	12	12	12	mA	1, 2, 3
I _{DD6ET}	All	15	15	15	15	mA	2, 4
I _{DD7}	x4, 8	121	150	156	164	mA	1, 2
	x16	152	172	195	219	mA	1, 2
I _{DD8}	All	I _{DD2P0} + 2mA	I _{DD2P0} + 2mA	I _{DD2P0} + 2mA	I _{DD2P0} + 2mA	mA	1, 2

- Notes:
1. T_C = 85°C; SRT and ASR are disabled.
 2. Enabling ASR could increase I_{DDx} by up to an additional 2mA.
 3. Restricted to T_C (MAX) = 85°C.
 4. T_C = 85°C; ASR and ODT are disabled; SRT is enabled.
 5. The I_{DD} values must be derated (increased) on IT-option devices when operated outside of the range 0°C ≤ T_C ≤ +85°C:
 - 5a. When T_C < 0°C: I_{DD2P0}, I_{DD2P1} and I_{DD3P} must be derated by 4%; I_{DD4R} and I_{DD4W} must be derated by 2%; and I_{DD6}, I_{DD6ET} and I_{DD7} must be derated by 7%.
 - 5b. When T_C > 85°C: I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, I_{DD4W}, and I_{DD5B} must be derated by 2%; I_{DD2Px} must be derated by 30%.

Electrical Specifications – DC and AC

DC Operating Conditions

Table 41: DDR3L 1.35V DC Electrical Characteristics and Operating Conditions

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Unit	Notes
Supply voltage	V_{DD}	1.283	1.35	1.45	V	1–7
I/O supply voltage	V_{DDQ}	1.283	1.35	1.45	V	1–7
Input leakage current Any input $0V \leq V_{IN} \leq V_{DD}$, V_{REF} pin $0V \leq V_{IN} \leq 1.1V$ (All other pins not under test = 0V)	I_I	–2	–	2	μA	
V_{REF} supply leakage current $V_{REFDQ} = V_{DD}/2$ or $V_{REFCA} = V_{DD}/2$ (All other pins not under test = 0V)	I_{VREF}	–1	–	1	μA	8, 9

- Notes:
1. V_{DD} and V_{DDQ} must track one another. V_{DDQ} must be $\leq V_{DD}$. $V_{SS} = V_{SSQ}$.
 2. V_{DD} and V_{DDQ} may include AC noise of $\pm 50mV$ (250 kHz to 20 MHz) in addition to the DC (0 Hz to 250 kHz) specifications. V_{DD} and V_{DDQ} must be at same level for valid AC timing parameters.
 3. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of $V_{DD}/V_{DDQ}(t)$ over a very long period of time (for example, 1 second).
 4. Under these supply voltages, the device operates to this DDR3L specification.
 5. If the maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
 6. Under 1.5V operation, this DDR3L device operates in accordance with the DDR3 specifications under the same speed timings as defined for this device.
 7. Once initialized for DDR3L operation, DDR3 operation may only be used if the device is in reset while V_{DD} and V_{DDQ} are changed for DDR3 operation (see VDD Voltage Switching (page 141)).
 8. The minimum limit requirement is for testing purposes. The leakage current on the V_{REF} pin should be minimal.
 9. V_{REF} (see Table 42).

Input Operating Conditions

Table 42: DDR3L 1.35V DC Electrical Characteristics and Input Conditions

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Nom	Max	Unit	Notes
V_{IN} low; DC/commands/address busses	V_{IL}	V_{SS}	N/A	See Table 43	V	
V_{IN} high; DC/commands/address busses	V_{IH}	See Table 43	N/A	V_{DD}	V	
Input reference voltage command/address bus	$V_{REFCA(DC)}$	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V	1, 2
I/O reference voltage DQ bus	$V_{REFDQ(DC)}$	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V	2, 3
I/O reference voltage DQ bus in SELF REFRESH	$V_{REFDQ(SR)}$	V_{SS}	$0.5 \times V_{DD}$	V_{DD}	V	4
Command/address termination voltage (system level, not direct DRAM input)	V_{TT}	–	$0.5 \times V_{DDQ}$	–	V	5

- Notes:
1. $V_{REFCA(DC)}$ is expected to be approximately $0.5 \times V_{DD}$ and to track variations in the DC level. Externally generated peak noise (non-common mode) on V_{REFCA} may not exceed $\pm 1\% \times V_{DD}$ around the $V_{REFCA(DC)}$ value. Peak-to-peak AC noise on V_{REFCA} should not exceed $\pm 2\%$ of $V_{REFCA(DC)}$.
 2. DC values are determined to be less than 20 MHz in frequency. DRAM must meet specifications if the DRAM induces additional AC noise greater than 20 MHz in frequency.
 3. $V_{REFDQ(DC)}$ is expected to be approximately $0.5 \times V_{DD}$ and to track variations in the DC level. Externally generated peak noise (non-common mode) on V_{REFDQ} may not exceed $\pm 1\% \times V_{DD}$ around the $V_{REFDQ(DC)}$ value. Peak-to-peak AC noise on V_{REFDQ} should not exceed $\pm 2\%$ of $V_{REFDQ(DC)}$.
 4. $V_{REFDQ(DC)}$ may transition to $V_{REFDQ(SR)}$ and back to $V_{REFDQ(DC)}$ when in SELF REFRESH, within restrictions outlined in the SELF REFRESH section.
 5. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors. Minimum and maximum values are system-dependent.

Table 43: DDR3L 1.35V Input Switching Conditions - Command and Address

Parameter/Condition	Symbol	DDR3L-800/1066	DDR3L-1333/1600	DDR3L-1866	Units
Command and Address					
Input high AC voltage: Logic 1	$V_{IH(AC160),min}^5$	160	160	–	mV
	$V_{IH(AC135),min}^5$	135	135	135	mV
	$V_{IH(AC125),min}^5$	–	–	125	mV
Input high DC voltage: Logic 1	$V_{IH(DC90),min}$	90	90	90	mV
Input low DC voltage: Logic 0	$V_{IL(DC90),min}$	–90	–90	–90	mV
Input low AC voltage: Logic 0	$V_{IL(AC125),min}^5$	–	–	–125	mV
	$V_{IL(AC135),min}^5$	–135	–135	–135	mV
	$V_{IL(AC160),min}^5$	–160	–160	–	mV
DQ and DM					
Input high AC voltage: Logic 1	$V_{IH(AC160),min}^5$	160	160	–	mV
	$V_{IH(AC135),min}^5$	135	135	135	mV
	$V_{IH(AC125),min}^5$	–	–	130	mV
Input high DC voltage: Logic 1	$V_{IH(DC90),min}$	90	90	90	mV
Input low DC voltage: Logic 0	$V_{IL(DC90),min}$	–90	–90	–90	mV
Input low AC voltage: Logic 0	$V_{IL(AC125),min}^5$	–	–	–130	mV
	$V_{IL(AC135),min}^5$	–135	–135	–135	mV
	$V_{IL(AC160),min}^5$	–160	–160	–	mV

- Notes:
1. All voltages are referenced to V_{REF} . V_{REF} is V_{REFCA} for control, command, and address. All slew rates and setup/hold times are specified at the DRAM ball. V_{REF} is V_{REFDQ} for DQ and DM inputs.
 2. Input setup timing parameters (t_{IS} and t_{DS}) are referenced at $V_{IL(AC)}/V_{IH(AC)}$, not $V_{REF(DC)}$.
 3. Input hold timing parameters (t_{IH} and t_{DH}) are referenced at $V_{IL(DC)}/V_{IH(DC)}$, not $V_{REF(DC)}$.
 4. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).
 5. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

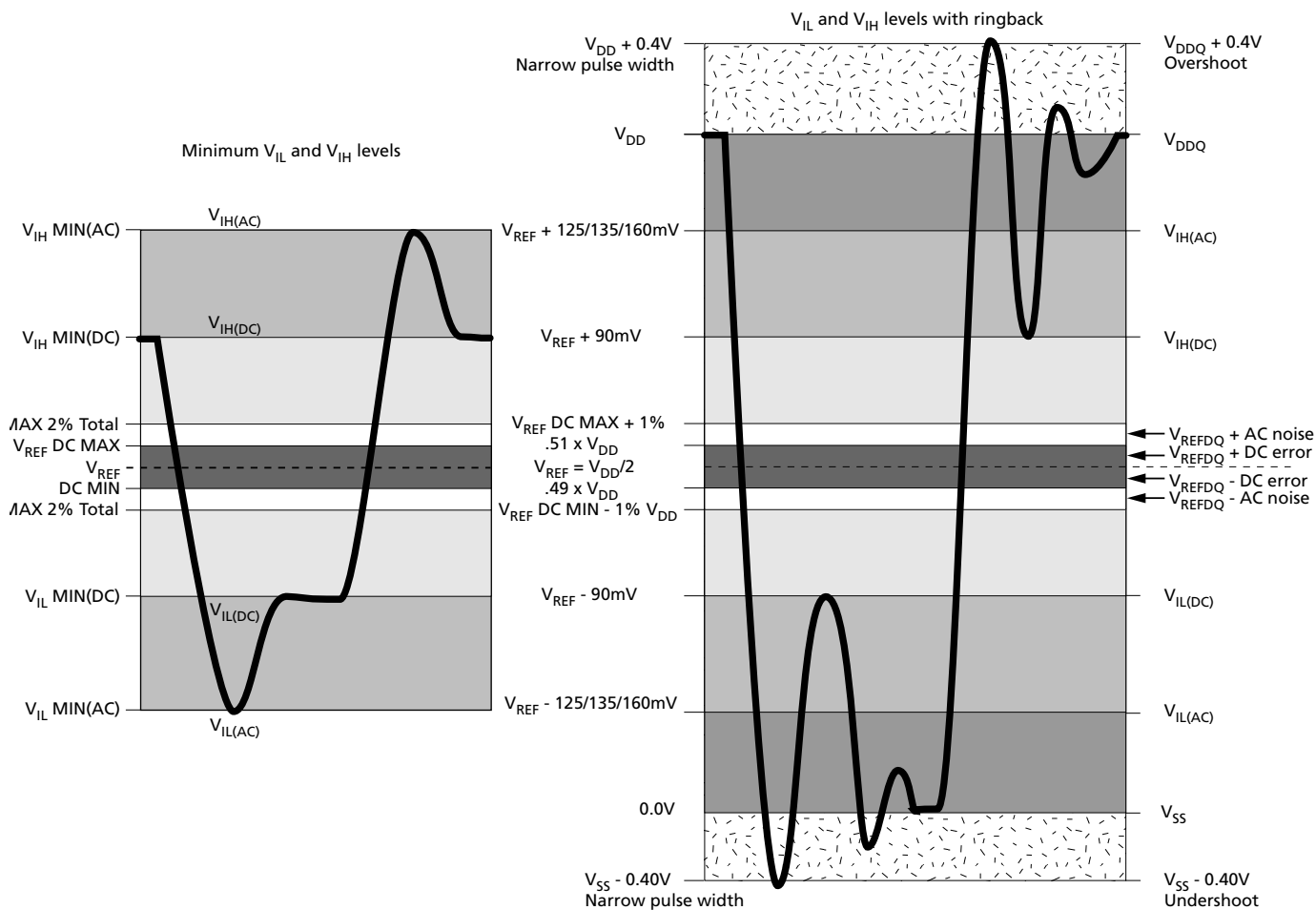
For example, for DDR3-800, two input AC levels are defined: $V_{IH(AC160),min}$ and $V_{IH(AC135),min}$ (corresponding $V_{IL(AC160),min}$ and $V_{IL(AC135),min}$). For DDR3-800, the address/command inputs must use either $V_{IH(AC160),min}$ with $t_{IS(AC160)}$ of 210ps or $V_{IH(AC150),min}$ with $t_{IS(AC135)}$ of 365ps; independently, the data inputs must use either $V_{IH(AC160),min}$ with $t_{DS(AC160)}$ of 75ps or $V_{IH(AC150),min}$ with $t_{DS(AC150)}$ of 125ps.

Table 44: DDR3L 1.35V Differential Input Operating Conditions (CK, CK# and DQS, DQS#)

Parameter/Condition	Symbol	Min	Max	Units	Notes
Differential input logic high – slew	$V_{IH,diff(AC)slew}$	180	N/A	mV	4
Differential input logic low – slew	$V_{IL,diff(AC)slew}$	N/A	-180	mV	4
Differential input logic high	$V_{IH,diff(AC)}$	$2 \times (V_{IH(AC)} - V_{REF})$	V_{DD}/V_{DDQ}	mV	5
Differential input logic low	$V_{IL,diff(AC)}$	V_{SS}/V_{SSQ}	$2 \times (V_{IL(AC)} - V_{REF})$	mV	6
Differential input crossing voltage relative to $V_{DD}/2$ for DQS, DQS#; CK, CK#	V_{IX}	$V_{REF(DC)} - 150$	$V_{REF(DC)} + 150$	mV	5, 7, 9
Differential input crossing voltage relative to $V_{DD}/2$ for CK, CK#	$V_{IX} (175)$	$V_{REF(DC)} - 175$	$V_{REF(DC)} + 175$	mV	5, 7–9
Single-ended high level for strobes	V_{SEH}	$V_{DDQ}/2 + 160$	V_{DDQ}	mV	5
Single-ended high level for CK, CK#		$V_{DD}/2 + 160$	V_{DD}	mV	5
Single-ended low level for strobes	V_{SEL}	V_{SSQ}	$V_{DDQ}/2 - 160$	mV	6
Single-ended low level for CK, CK#		V_{SS}	$V_{DD}/2 - 160$	mV	6

- Notes:
1. Clock is referenced to V_{DD} and V_{SS} . Data strobe is referenced to V_{DDQ} and V_{SSQ} .
 2. Reference is $V_{REFCA(DC)}$ for clock and $V_{REFDQ(DC)}$ for strobe.
 3. Differential input slew rate = 2 V/ns.
 4. Defines slew rate reference points, relative to input crossing voltages.
 5. Minimum DC limit is relative to single-ended signals; overshoot specifications are applicable.
 6. Maximum DC limit is relative to single-ended signals; undershoot specifications are applicable.
 7. The typical value of $V_{IX(AC)}$ is expected to be about $0.5 \times V_{DD}$ of the transmitting device, and $V_{IX(AC)}$ is expected to track variations in V_{DD} . $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.
 8. The V_{IX} extended range (± 175 mV) is allowed only for the clock; this V_{IX} extended range is only allowed when the following conditions are met: The single-ended input signals are monotonic, have the single-ended swing V_{SEL} , V_{SEH} of at least $V_{DD}/2 \pm 250$ mV, and the differential slew rate of CK, CK# is greater than 3 V/ns.
 9. V_{IX} must provide 25mV (single-ended) of the voltages separation.

Figure 11: DDR3L 1.35V Input Signal



Note: 1. Numbers in diagrams reflect nominal values.

DDR3L 1.35V AC Overshoot/Undershoot Specification

Table 45: DDR3L Control and Address Pins

Parameter	DDR3L-800	DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866
Maximum peak amplitude allowed for overshoot area (see Figure 12)	0.4V	0.4V	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure 13)	0.4V	0.4V	0.4V	0.4V	0.4V
Maximum overshoot area above V_{DD} (see Figure 12)	0.67 Vns	0.5 Vns	0.4 Vns	0.33 Vns	0.28 Vns
Maximum undershoot area below V_{SS} (see Figure 13)	0.67 Vns	0.5 Vns	0.4 Vns	0.33 Vns	0.28 Vns

Table 46: DDR3L 1.35V Clock, Data, Strobe, and Mask Pins

Parameter	DDR3L-800	DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866
Maximum peak amplitude allowed for overshoot area (see Figure 12)	0.4V	0.4V	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure 13)	0.4V	0.4V	0.4V	0.4V	0.4V
Maximum overshoot area above V_{DD}/V_{DDQ} (see Figure 12)	0.25 Vns	0.19 Vns	0.15 Vns	0.13 Vns	0.11 Vns
Maximum undershoot area below V_{SS}/V_{SSQ} (see Figure 13)	0.25 Vns	0.19 Vns	0.15 Vns	0.13 Vns	0.11 Vns

Figure 12: Overshoot

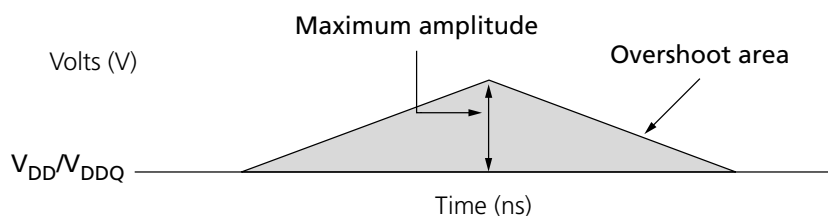


Figure 13: Undershoot

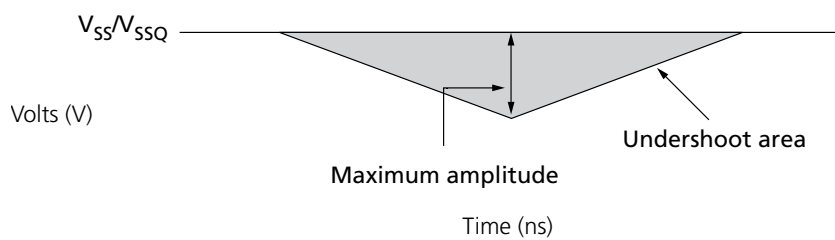


Figure 14: V_{IX} for Differential Signals

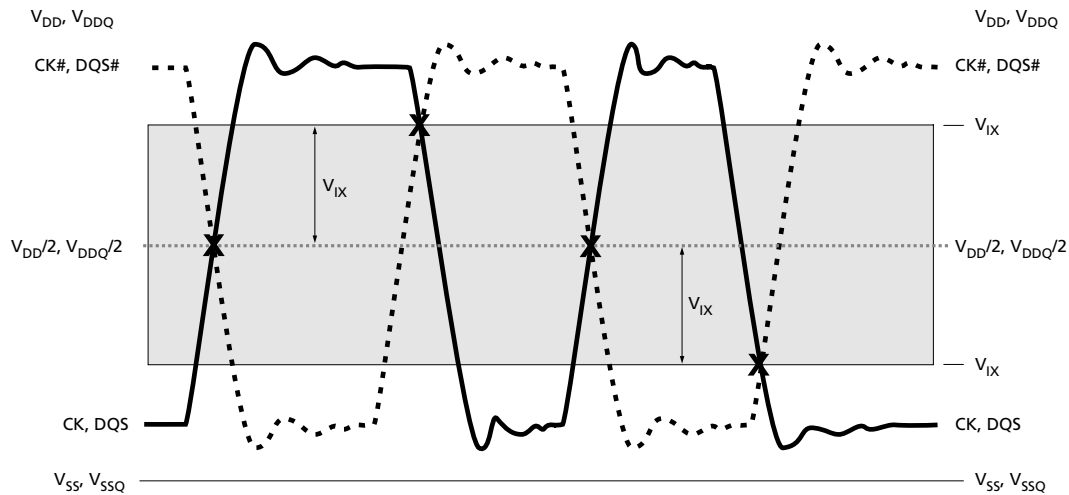


Figure 15: Single-Ended Requirements for Differential Signals

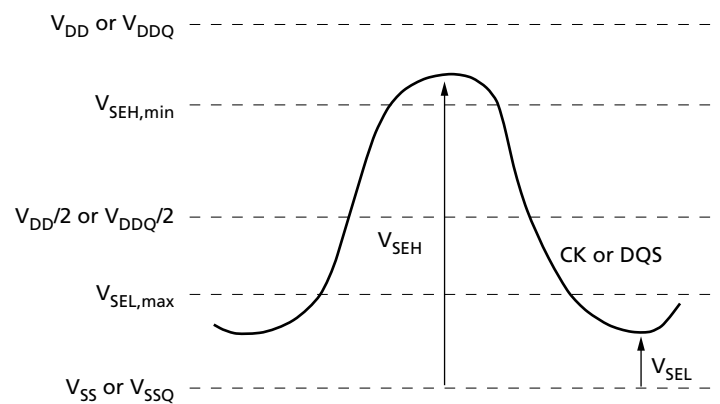
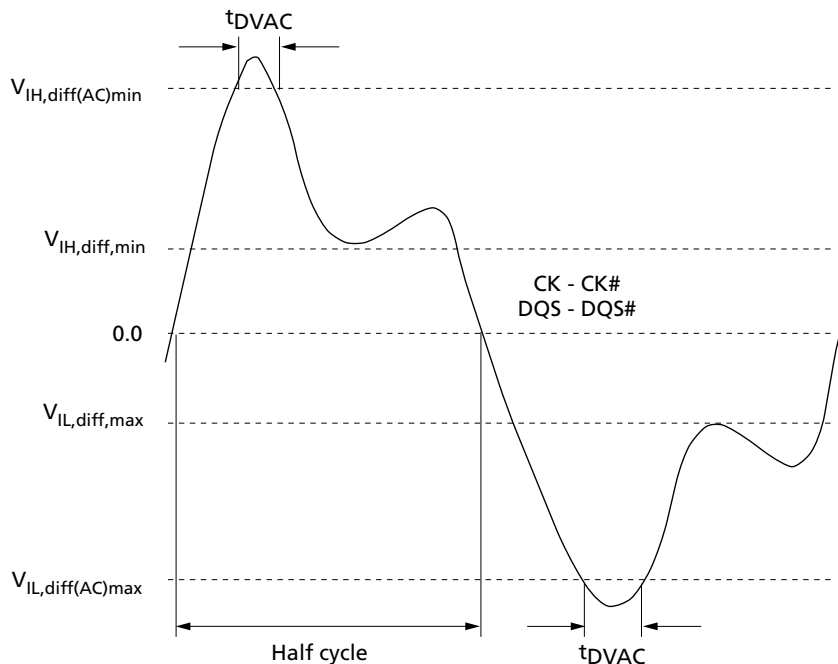


Figure 16: Definition of Differential AC-Swing and t_{DVAC}

Table 47: DDR3L 1.35V - Minimum Required Time t_{DVAC} for CK/CK#, DQS/DQS# Differential for AC Ringback

Slew Rate (V/ns)	DDR3L-800/1066/1333/1600		DDR3L-1866		
	t_{DVAC} at 320mV (ps)	t_{DVAC} at 270mV (ps)	t_{DVAC} at 270mV (ps)	t_{DVAC} at 250mV (ps)	t_{DVAC} at 260mV (ps)
>4.0	189	201	163	168	176
4.0	189	201	163	168	176
3.0	162	179	140	147	154
2.0	109	134	95	105	111
1.8	91	119	80	91	97
1.6	69	100	62	74	78
1.4	40	76	37	52	55
1.2	Note1	44	5	22	24
1.0	Note1				
<1.0	Note1				

Note: 1. Rising input signal shall become equal to or greater than $V_{IH(AC)}$ level and Falling input signal shall become equal to or less than $V_{IL(AC)}$ level.

DDR3L 1.35V Slew Rate Definitions for Single-Ended Input Signals

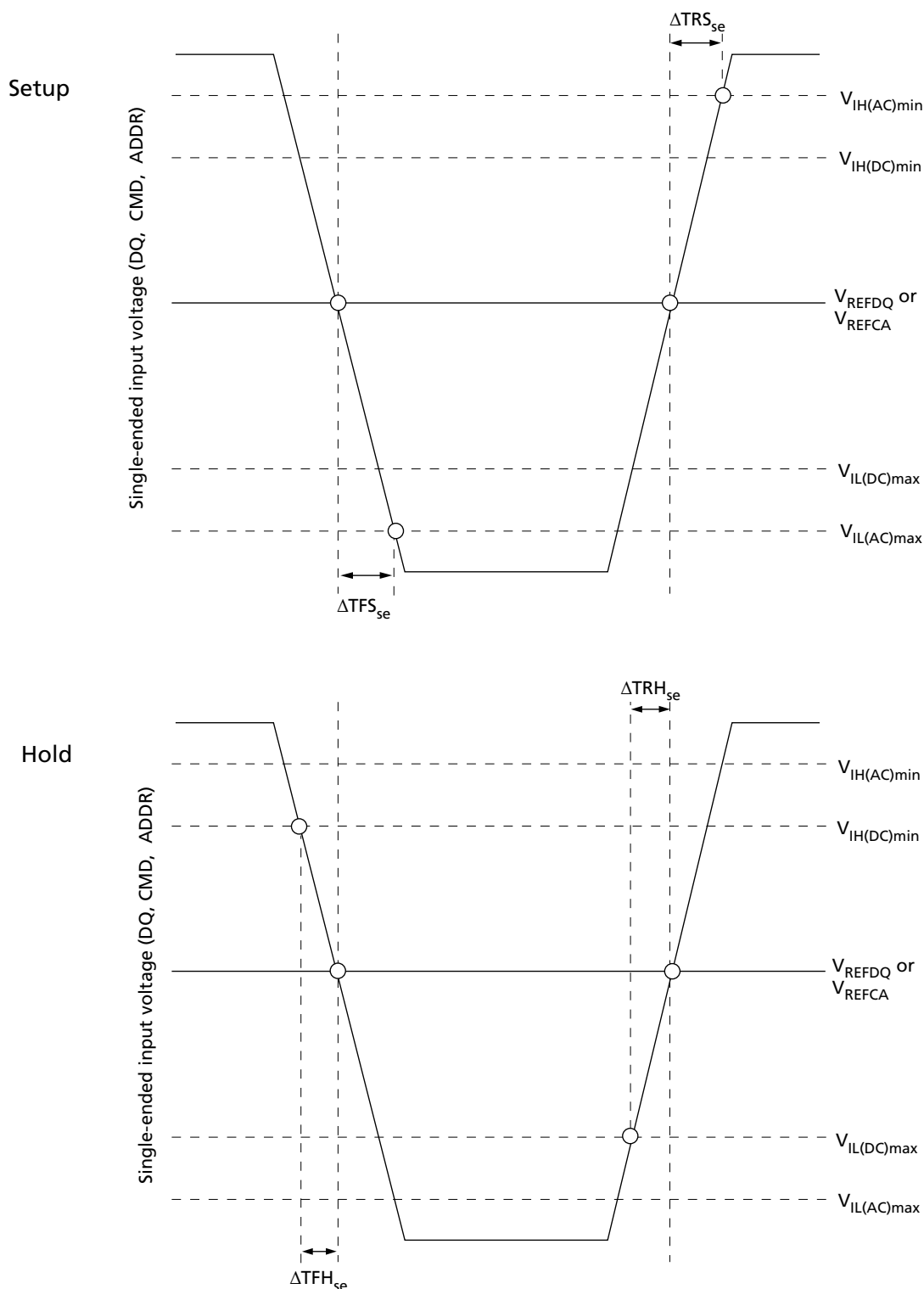
Setup (t_{IS} and t_{DS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{REF} and the first crossing of $V_{IH(AC),min}$. Setup (t_{IS} and t_{DS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{REF} and the first crossing of $V_{IL(AC),max}$.

Hold (t_{IH} and t_{DH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC),max}$ and the first crossing of V_{REF} . Hold (t_{IH} and t_{DH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC),min}$ and the first crossing of V_{REF} (see Figure 17 (page 62)).

Table 48: Single-Ended Input Slew Rate Definition

Input Slew Rates (Linear Signals)		Measured		Calculation
Input	Edge	From	To	
Setup	Rising	V_{REF}	$V_{IH(AC),min}$	$\frac{V_{IH(AC),min} - V_{REF}}{\Delta TRS_{se}}$
	Falling	V_{REF}	$V_{IL(AC),max}$	$\frac{V_{REF} - V_{IL(AC),max}}{\Delta TFS_{se}}$
Hold	Rising	$V_{IL(DC),max}$	V_{REF}	$\frac{V_{REF} - V_{IL(DC),max}}{\Delta TFH_{se}}$
	Falling	$V_{IH(DC),min}$	V_{REF}	$\frac{V_{IH(DC),min} - V_{REF}}{\Delta TRSH_{se}}$

Figure 17: Nominal Slew Rate Definition for Single-Ended Input Signals



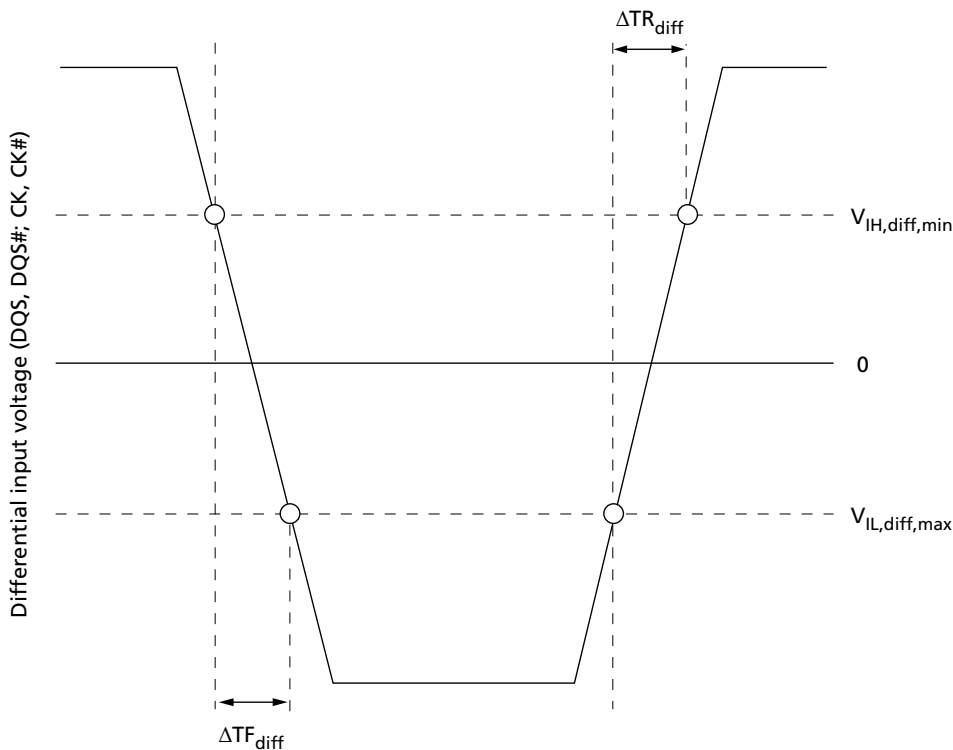
DDR3L 1.35V Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, CK# and DQS, DQS#) are defined and measured, as shown in Table 49 and Figure 18. The nominal slew rate for a rising signal is defined as the slew rate between $V_{IL,diff,max}$ and $V_{IH,diff,min}$. The nominal slew rate for a falling signal is defined as the slew rate between $V_{IH,diff,min}$ and $V_{IL,diff,max}$.

Table 49: DDR3L 1.35V Differential Input Slew Rate Definition

Differential Input Slew Rates (Linear Signals)		Measured		Calculation
Input	Edge	From	To	
CK and DQS reference	Rising	$V_{IL,diff,max}$	$V_{IH,diff,min}$	$\frac{V_{IH,diff,min} - V_{IL,diff,max}}{\Delta TR_{diff}}$
	Falling	$V_{IH,diff,min}$	$V_{IL,diff,max}$	$\frac{V_{IH,diff,min} - V_{IL,diff,max}}{\Delta TF_{diff}}$

Figure 18: DDR3L 1.35V Nominal Differential Input Slew Rate Definition for DQS, DQS# and CK, CK#



ODT Characteristics

The ODT effective resistance R_{TT} is defined by MR1 [9, 6, and 2]. ODT is applied to the DQ, DM, DQS, DQS#, and TDQS, TDQS# balls (x8 devices only). The ODT target values and a functional representation are listed in Table 50 and Table 51 (page 65). The individual pull-up and pull-down resistors ($R_{TT(PU)}$ and $R_{TT(PD)}$) are defined as follows:

- $R_{TT(PU)} = (V_{DDQ} - V_{OUT}) / |I_{OUT}|$, under the condition that $R_{TT(PD)}$ is turned off
- $R_{TT(PD)} = (V_{OUT}) / |I_{OUT}|$, under the condition that $R_{TT(PU)}$ is turned off

Figure 19: ODT Levels and I-V Characteristics

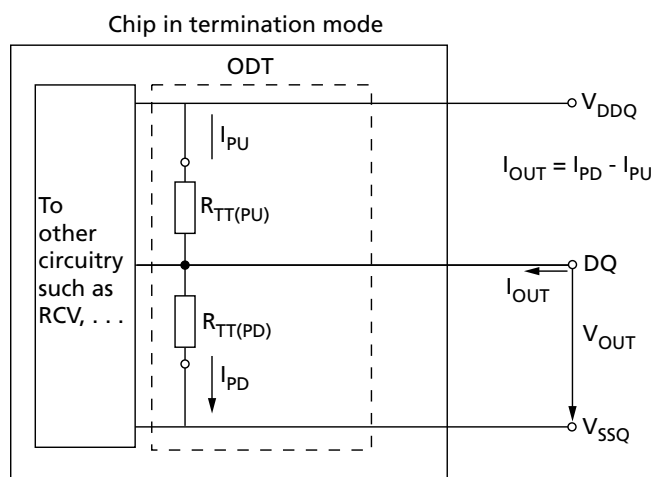


Table 50: On-Die Termination DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Nom	Max	Unit	Notes
R_{TT} effective impedance	$R_{TT(EFF)}$	See Table 51 (page 65)				1, 2
Deviation of VM with respect to $V_{DDQ}/2$	ΔVM	-5		5	%	1, 2, 3

Notes: 1. Tolerance limits are applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$, $V_{SSQ} = V_{SS}$). Refer to ODT Sensitivity (page 66) if either the temperature or voltage changes after calibration.

2. Measurement definition for R_{TT} : Apply $V_{IH(AC)}$ to pin under test and measure current $I[V_{IH(AC)}]$, then apply $V_{IL(AC)}$ to pin under test and measure current $I[V_{IL(AC)}]$:

$$R_{TT} = \frac{V_{IH(AC)} - V_{IL(AC)}}{I(V_{IH(AC)}) - I(V_{IL(AC)})}$$

3. Measure voltage (VM) at the tested pin with no load:

$$\Delta VM = \left(\frac{2 \times VM}{V_{DDQ}} - 1 \right) \times 100$$

4. For IT and AT devices, the minimum values are derated by 6% when the device operates between -40°C and 0°C (T_C).

1.35V ODT Resistors

Table 51 provides an overview of the ODT DC electrical characteristics. The values provided are not specification requirements; however, they can be used as design guidelines to indicate what R_{TT} is targeted to provide:

- R_{TT} 120Ω is made up of $R_{TT120(PD240)}$ and $R_{TT120(PU240)}$
- R_{TT} 60Ω is made up of $R_{TT60(PD120)}$ and $R_{TT60(PU120)}$
- R_{TT} 40Ω is made up of $R_{TT40(PD80)}$ and $R_{TT40(PU80)}$
- R_{TT} 30Ω is made up of $R_{TT30(PD60)}$ and $R_{TT30(PU60)}$
- R_{TT} 20Ω is made up of $R_{TT20(PD40)}$ and $R_{TT20(PU40)}$

Table 51: 1.35V R_{TT} Effective Impedance

MR1 [9, 6, 2]	R _{TT}	Resistor	V _{OUT}	Min	Nom	Max	Units
0, 1, 0	120Ω	R _{TT,120PD240}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/1
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/1
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/1
		R _{TT,120PU240}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/1
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/1
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/1
	120Ω		V _{IL(AC)} to V _{IH(AC)}	0.9	1.0	1.65	RZQ/2
0, 0, 1	60Ω	R _{TT,60PD120}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/2
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/2
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/2
		R _{TT,60PU120}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/2
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/2
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/2
	60Ω		V _{IL(AC)} to V _{IH(AC)}	0.9	1.0	1.65	RZQ/4
0, 1, 1	40Ω	R _{TT,40PD80}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/3
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/3
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/3
		R _{TT,40PU80}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/3
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/3
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/3
	40Ω		V _{IL(AC)} to V _{IH(AC)}	0.9	1.0	1.65	RZQ/6
1, 0, 1	30Ω	R _{TT,30PD60}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/4
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/4
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/4
		R _{TT,30PU60}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/4
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/4
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/4
	30Ω		V _{IL(AC)} to V _{IH(AC)}	0.9	1.0	1.65	RZQ/8

Table 51: 1.35V R_{TT} Effective Impedance (Continued)

MR1 [9, 6, 2]	R_{TT}	Resistor	V_{OUT}	Min	Nom	Max	Units
1, 0, 0	20 Ω	$R_{TT,20PD40}$	$0.2 \times V_{DDQ}$	0.6	1.0	1.15	RZQ/6
			$0.5 \times V_{DDQ}$	0.9	1.0	1.15	RZQ/6
			$0.8 \times V_{DDQ}$	0.9	1.0	1.45	RZQ/6
		$R_{TT,20PU40}$	$0.2 \times V_{DDQ}$	0.9	1.0	1.45	RZQ/6
			$0.5 \times V_{DDQ}$	0.9	1.0	1.15	RZQ/6
			$0.8 \times V_{DDQ}$	0.6	1.0	1.15	RZQ/6
	20 Ω	$V_{IL(AC)}$ to $V_{IH(AC)}$		0.9	1.0	1.65	RZQ/12

ODT Sensitivity

If either the temperature or voltage changes after I/O calibration, then the tolerance limits listed in Table 50 and Table 51 can be expected to widen according to Table 52 and Table 53.

Table 52: ODT Sensitivity Definition

Symbol	Min	Max	Unit
R_{TT}	$0.9 - dR_{TT}dT \times DT - dR_{TT}dV \times DV $	$1.6 + dR_{TT}dT \times DT + dR_{TT}dV \times DV $	RZQ/(2, 4, 6, 8, 12)

Note: 1. $\Delta T = T - T(\text{@ calibration})$, $\Delta V = V_{DDQ} - V_{DDQ}(\text{@ calibration})$ and $V_{DD} = V_{DDQ}$.

Table 53: ODT Temperature and Voltage Sensitivity

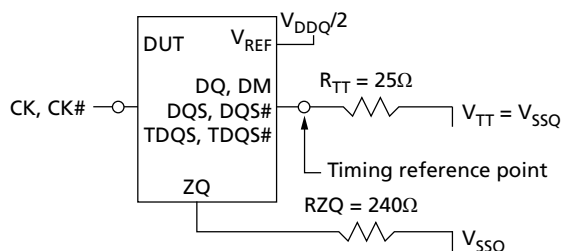
Change	Min	Max	Unit
$dR_{TT}dT$	0	1.5	%/ $^{\circ}\text{C}$
$dR_{TT}dV$	0	0.15	%/mV

Note: 1. $\Delta T = T - T(\text{@ calibration})$, $\Delta V = V_{DDQ} - V_{DDQ}(\text{@ calibration})$ and $V_{DD} = V_{DDQ}$.

ODT Timing Definitions

ODT loading differs from that used in AC timing measurements. The reference load for ODT timings is shown in Figure 20. Two parameters define when ODT turns on or off synchronously, two define when ODT turns on or off asynchronously, and another defines when ODT turns on or off dynamically. Table 54 and Table 55 (page 67) outline and provide definition and measurement references settings for each parameter.

ODT turn-on time begins when the output leaves High-Z and ODT resistance begins to turn on. ODT turn-off time begins when the output leaves Low-Z and ODT resistance begins to turn off.

Figure 20: ODT Timing Reference Load

Table 54: ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition	Figure
t_{AON}	Rising edge of CK – CK# defined by the end point of ODTL _{on}	Extrapolated point at V_{SSQ}	Figure 21 (page 68)
t_{AOF}	Rising edge of CK – CK# defined by the end point of ODTL _{off}	Extrapolated point at $V_{RTT,nom}$	Figure 21 (page 68)
t_{AONPD}	Rising edge of CK – CK# with ODT first being registered HIGH	Extrapolated point at V_{SSQ}	Figure 22 (page 68)
t_{AOFPD}	Rising edge of CK – CK# with ODT first being registered LOW	Extrapolated point at $V_{RTT,nom}$	Figure 22 (page 68)
t_{ADC}	Rising edge of CK – CK# defined by the end point of ODTL _{cnw} , ODTL _{cnw4} , or ODTL _{cnw8}	Extrapolated points at $V_{RTT(WR)}$ and $V_{RTT,nom}$	Figure 23 (page 69)

Table 55: DDR3L(1.35V) Reference Settings for ODT Timing Measurements

Measured Parameter	$R_{TT,nom}$ Setting	$R_{TT(WR)}$ Setting	V_{SW1}	V_{SW2}
t_{AON}	RZQ/4 (60Ω)	N/A	50mV	100mV
	RZQ/12 (20Ω)	N/A	100mV	200mV
t_{AOF}	RZQ/4 (60Ω)	N/A	50mV	100mV
	RZQ/12 (20Ω)	N/A	100mV	200mV
t_{AONPD}	RZQ/4 (60Ω)	N/A	50mV	100mV
	RZQ/12 (20Ω)	N/A	100mV	200mV
t_{AOFPD}	RZQ/4 (60Ω)	N/A	50mV	100mV
	RZQ/12 (20Ω)	N/A	100mV	200mV
t_{ADC}	RZQ/12 (20Ω)	RZQ/2 (20Ω)	200mV	250mV

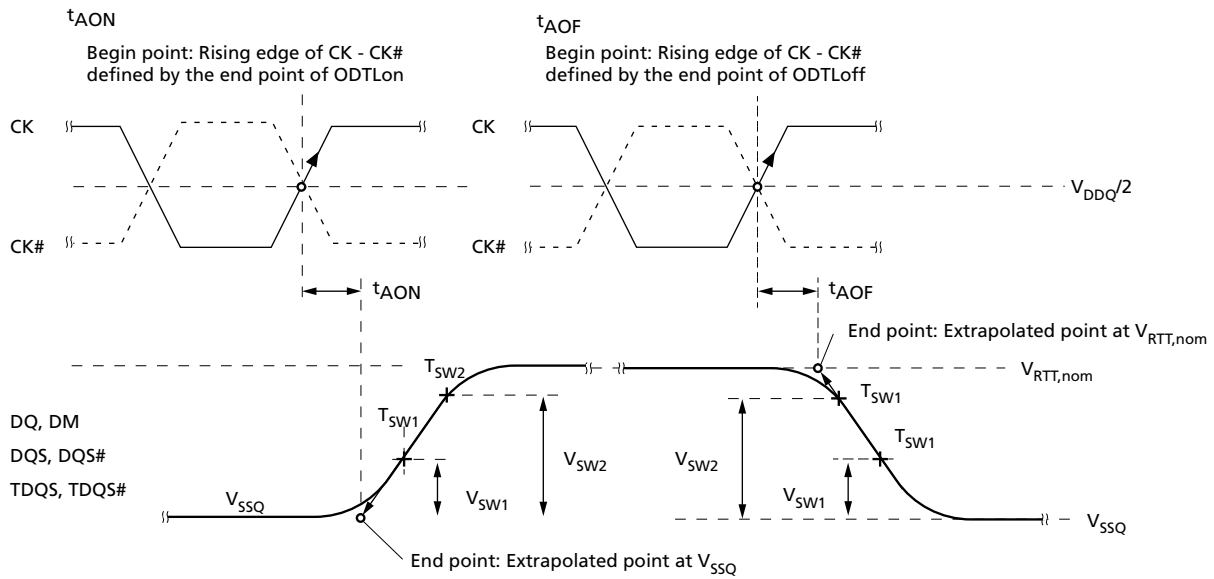
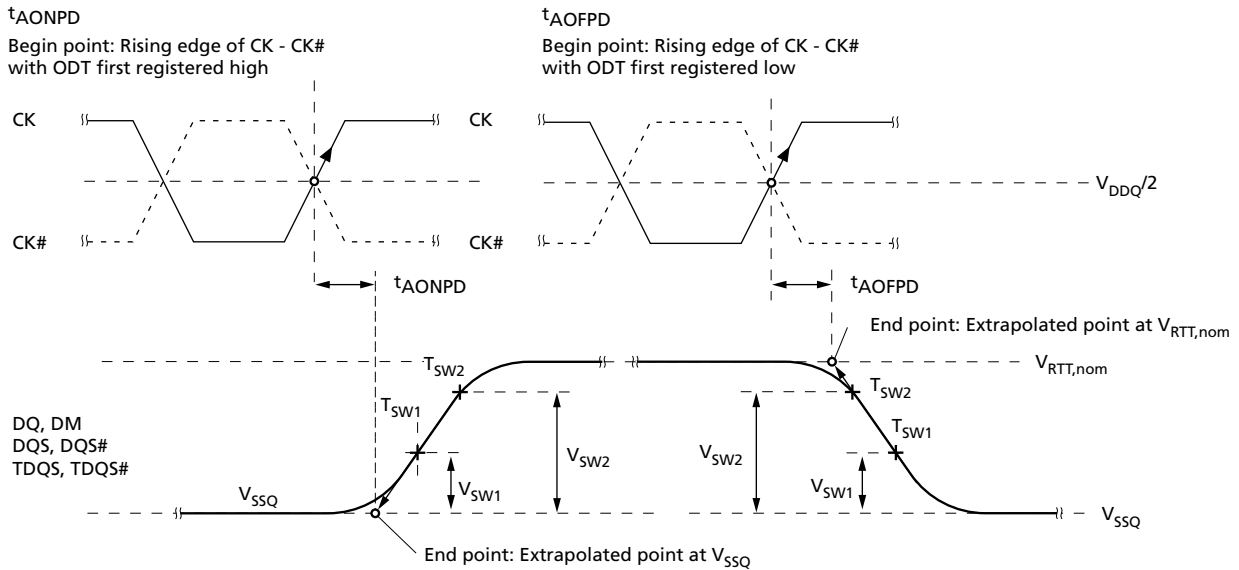
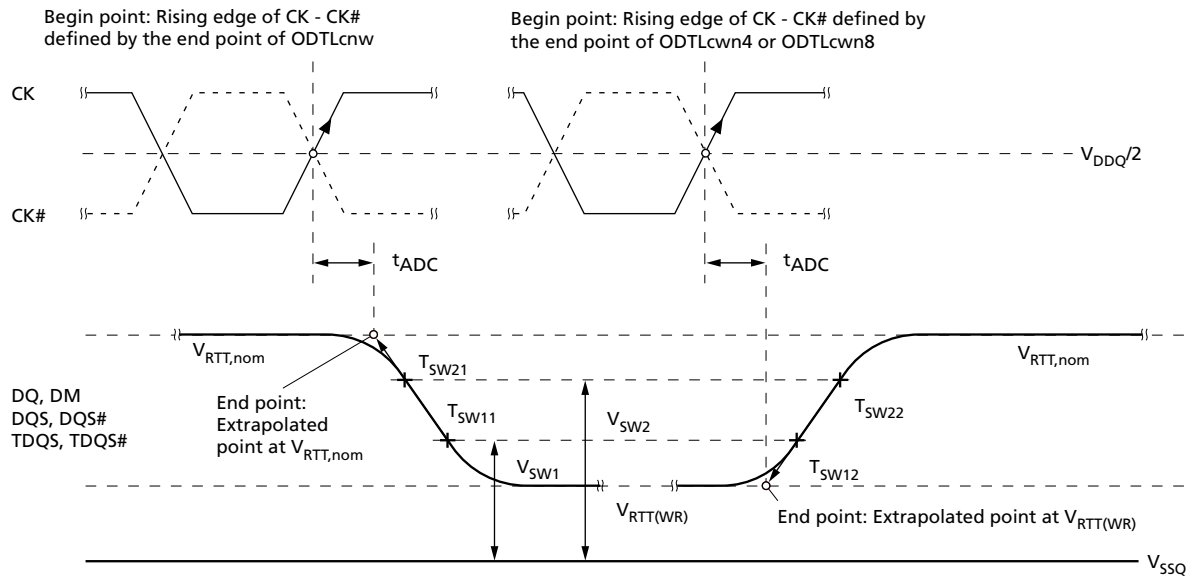
Figure 21: t_{AON} and t_{AOF} Definitions

Figure 22: t_{AONPD} and t_{AOFPD} Definitions


Figure 23: t_{ADC} Definition



Output Driver Impedance

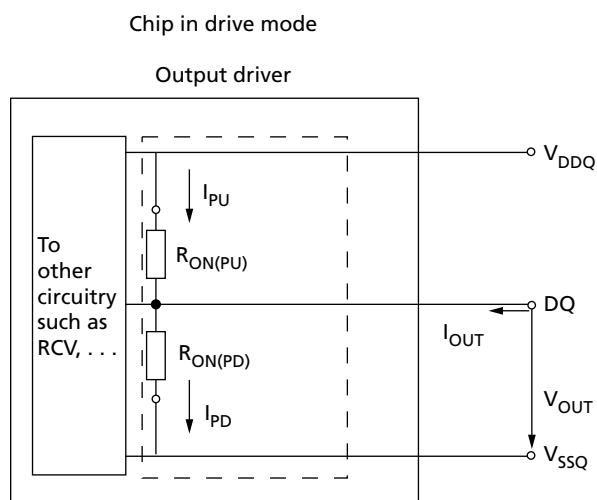
The output driver impedance is selected by MR1[5,1] during initialization. The selected value is able to maintain the tight tolerances specified if proper ZQ calibration is performed. Output specifications refer to the default output driver unless specifically stated otherwise. A functional representation of the output buffer is shown below. The output driver impedance R_{ON} is defined by the value of the external reference resistor RZQ as follows:

- $R_{ON,x} = RZQ/y$ (with $RZQ = 240\Omega \pm 1\%$; $x = 34\Omega$ or 40Ω with $y = 7$ or 6 , respectively)

The individual pull-up and pull-down resistors $R_{ON(PU)}$ and $R_{ON(PD)}$ are defined as follows:

- $R_{ON(PU)} = (V_{DDQ} - V_{OUT}) / |I_{OUT}|$, when $R_{ON(PD)}$ is turned off
- $R_{ON(PD)} = (V_{OUT}) / |I_{OUT}|$, when $R_{ON(PU)}$ is turned off

Figure 24: Output Driver



34 Ohm Output Driver Impedance

The 34Ω driver (MR1[5, 1] = 01) is the default driver. Unless otherwise stated, all timings and specifications listed herein apply to the 34Ω driver only. Its impedance R_{ON} is defined by the value of the external reference resistor RZQ as follows: $R_{ON34} = RZQ/7$ (with nominal RZQ = 240Ω ±1%) and is actually 34.3Ω ±1%.

Table 56: DDR3L 34 Ohm Driver Impedance Characteristics

MR1 [5, 1]	R _{ON}	Resistor	V _{OUT}	Min	Nom	Max	Units
0, 1	34.3Ω	R _{ON,34PD}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/7
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/7
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/7
		R _{ON,34PU}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/7
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/7
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/7
Pull-up/pull-down mismatch (MM _{PUPD})			V _{IL(AC)} to V _{IH(AC)}	−10	N/A	10	%

- Notes:
1. Tolerance limits assume RZQ of 240Ω ±1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage: $V_{DDQ} = V_{DD}$; $V_{SSQ} = V_{SS}$. Refer to DDR3L 34 Ohm Output Driver Sensitivity (page 73) if either the temperature or the voltage changes after calibration.
 2. Measurement definition for mismatch between pull-up and pull-down (MM_{PUPD}). Measure both $R_{ON(PU)}$ and $R_{ON(PD)}$ at $0.5 \times V_{DDQ}$:

$$MM_{PUPD} = \frac{R_{ON(PU)} - R_{ON(PD)}}{R_{ON,nom}} \times 100$$
 3. For IT and AT devices, the minimum values are derated by 6% when the device operates between -40°C and 0°C (T_C).
A larger maximum limit will result in slightly lower minimum currents.

DDR3L 34 Ohm Driver

Using Table 57, the 34Ω driver's current range has been calculated and summarized in Table 58 (page 72) $V_{DD} = 1.35V$, Table 59 for $V_{DD} = 1.45V$, and Table 60 (page 73) for $V_{DD} = 1.283V$. The individual pull-up and pull-down resistors $R_{ON34(PD)}$ and $R_{ON34(PU)}$ are defined as follows:

- $R_{ON34(PD)} = (V_{OUT}) / |I_{OUT}|$; $R_{ON34(PU)}$ is turned off
- $R_{ON34(PU)} = (V_{DDQ} - V_{OUT}) / |I_{OUT}|$; $R_{ON34(PD)}$ is turned off

Table 57: DDR3L 34 Ohm Driver Pull-Up and Pull-Down Impedance Calculations

R_{ON}				Min	Nom	Max	Unit
$RZQ = 240\Omega \pm 1\%$				237.6	240	242.4	Ω
$RZQ/7 = (240\Omega \pm 1\%)/7$				33.9	34.3	34.6	Ω
MR1[5,1]	R_{ON}	Resistor	V_{OUT}	Min	Nom	Max	Unit
0, 1	34.3Ω	$R_{ON34(PD)}$	$0.2 \times V_{DDQ}$	20.4	34.3	38.1	Ω
			$0.5 \times V_{DDQ}$	30.5	34.3	38.1	Ω
			$0.8 \times V_{DDQ}$	30.5	34.3	48.5	Ω
		$R_{ON34(PU)}$	$0.2 \times V_{DDQ}$	30.5	34.3	48.5	Ω
			$0.5 \times V_{DDQ}$	30.5	34.3	38.1	Ω
			$0.8 \times V_{DDQ}$	20.4	34.3	38.1	Ω

Table 58: DDR3L 34 Ohm Driver I_{OH}/I_{OL} Characteristics: $V_{DD} = V_{DDQ} = \text{DDR3L@1.35V}$

MR1[5,1]	R_{ON}	Resistor	V_{OUT}	Max	Nom	Min	Unit
0, 1	34.3Ω	$R_{ON34(PD)}$	$I_{OL} @ 0.2 \times V_{DDQ}$	13.3	7.9	7.1	mA
			$I_{OL} @ 0.5 \times V_{DDQ}$	22.1	19.7	17.7	mA
			$I_{OL} @ 0.8 \times V_{DDQ}$	35.4	31.5	22.3	mA
		$R_{ON34(PU)}$	$I_{OH} @ 0.2 \times V_{DDQ}$	35.4	31.5	22.3	mA
			$I_{OH} @ 0.5 \times V_{DDQ}$	22.1	19.7	17.7	mA
			$I_{OH} @ 0.8 \times V_{DDQ}$	13.3	7.9	7.1	mA

Table 59: DDR3L 34 Ohm Driver I_{OH}/I_{OL} Characteristics: $V_{DD} = V_{DDQ} = \text{DDR3L@1.45V}$

MR1[5,1]	R_{ON}	Resistor	V_{OUT}	Max	Nom	Min	Unit
0, 1	34.3Ω	$R_{ON34(PD)}$	$I_{OL} @ 0.2 \times V_{DDQ}$	14.2	8.5	7.6	mA
			$I_{OL} @ 0.5 \times V_{DDQ}$	23.7	21.1	19.0	mA
			$I_{OL} @ 0.8 \times V_{DDQ}$	38.0	33.8	23.9	mA
		$R_{ON34(PU)}$	$I_{OH} @ 0.2 \times V_{DDQ}$	38.0	33.8	23.9	mA
			$I_{OH} @ 0.5 \times V_{DDQ}$	23.7	21.1	19.0	mA
			$I_{OH} @ 0.8 \times V_{DDQ}$	14.2	8.5	7.6	mA

Table 60: DDR3L 34 Ohm Driver I_{OH}/I_{OL} Characteristics: $V_{DD} = V_{DDQ} = \text{DDR3L@1.283}$

MR1[5,1]	R_{ON}	Resistor	V_{OUT}	Max	Nom	Min	Unit
0, 1	34.3Ω	$R_{ON34(PD)}$	$I_{OL} @ 0.2 \times V_{DDQ}$	12.6	7.5	6.7	mA
			$I_{OL} @ 0.5 \times V_{DDQ}$	21.0	18.7	16.8	mA
			$I_{OL} @ 0.8 \times V_{DDQ}$	33.6	29.9	21.2	mA
		$R_{ON34(PU)}$	$I_{OH} @ 0.2 \times V_{DDQ}$	33.6	29.9	21.2	mA
			$I_{OH} @ 0.5 \times V_{DDQ}$	21.0	18.7	16.8	mA
			$I_{OH} @ 0.8 \times V_{DDQ}$	12.6	7.5	6.7	mA

DDR3L 34 Ohm Output Driver Sensitivity

If either the temperature or the voltage changes after ZQ calibration, then the tolerance limits listed in Table 56 (page 71) can be expected to widen according to Table 61 and Table 62.

Table 61: DDR3L 34 Ohm Output Driver Sensitivity Definition

Symbol	Min	Max	Unit
$R_{ON(PD)} @ 0.2 \times V_{DDQ}$	$0.6 - dR_{ONdTL} \times \Delta T - dR_{ONdVL} \times \Delta V $	$1.1 + dR_{ONdTL} \times \Delta T + dR_{ONdVL} \times \Delta V $	RZQ/7
$R_{ON(PD)} @ 0.5 \times V_{DDQ}$	$0.9 - dR_{ONdTM} \times \Delta T - dR_{ONdVM} \times \Delta V $	$1.1 + dR_{ONdTM} \times \Delta T + dR_{ONdVM} \times \Delta V $	RZQ/7
$R_{ON(PD)} @ 0.8 \times V_{DDQ}$	$0.9 - dR_{ONdTH} \times \Delta T - dR_{ONdVH} \times \Delta V $	$1.4 + dR_{ONdTH} \times \Delta T + dR_{ONdVH} \times \Delta V $	RZQ/7
$R_{ON(PU)} @ 0.2 \times V_{DDQ}$	$0.9 - dR_{ONdTL} \times \Delta T - dR_{ONdVL} \times \Delta V $	$1.4 + dR_{ONdTL} \times \Delta T + dR_{ONdVL} \times \Delta V $	RZQ/7
$R_{ON(PU)} @ 0.5 \times V_{DDQ}$	$0.9 - dR_{ONdTM} \times \Delta T - dR_{ONdVM} \times \Delta V $	$1.1 + dR_{ONdTM} \times \Delta T + dR_{ONdVM} \times \Delta V $	RZQ/7
$R_{ON(PU)} @ 0.8 \times V_{DDQ}$	$0.6 - dR_{ONdTH} \times \Delta T - dR_{ONdVH} \times \Delta V $	$1.1 + dR_{ONdTH} \times \Delta T + dR_{ONdVH} \times \Delta V $	RZQ/7

Note: 1. $\Delta T = T - T_{(CALIBRATION)}$; $\Delta V = V_{DDQ} - V_{DDQ(CALIBRATION)}$; and $V_{DD} = V_{DDQ}$.

Table 62: DDR3L 34 Ohm Output Driver Voltage and Temperature Sensitivity

Change	Min	Max	Unit
dR_{ONdTM}	0	1.5	%/°C
dR_{ONdVM}	0	0.13	%/mV
dR_{ONdTL}	0	1.5	%/°C
dR_{ONdVL}	0	0.13	%/mV
dR_{ONdTH}	0	1.5	%/°C
dR_{ONdVH}	0	0.13	%/mV

DDR3L Alternative 40 Ohm Driver

Table 63: DDR3L 40 Ohm Driver Impedance Characteristics

MR1 [5, 1]	R _{ON}	Resistor	V _{OUT}	Min	Nom	Max	Units
0, 0	40Ω	R _{ON,40PD}	0.2 × V _{DDQ}	0.6	1.0	1.15	RZQ/6
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V _{DDQ}	0.9	1.0	1.45	RZQ/6
		R _{ON,40PU}	0.2 × V _{DDQ}	0.9	1.0	1.45	RZQ/6
			0.5 × V _{DDQ}	0.9	1.0	1.15	RZQ/6
			0.8 × V _{DDQ}	0.6	1.0	1.15	RZQ/6
Pull-up/pull-down mismatch (MM _{PUPD})		V _{IL(AC)} to V _{IH(AC)}	−10	N/A	10	%	

- Notes:
1. Tolerance limits assume RZQ of 240Ω ±1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage (V_{DDQ} = V_{DD}; V_{SSQ} = V_{SS}). Refer to DDR3L 40 Ohm Output Driver Sensitivity (page 74) if either the temperature or the voltage changes after calibration.
 2. Measurement definition for mismatch between pull-up and pull-down (MM_{PUPD}). Measure both R_{ON(PU)} and R_{ON(PD)} at 0.5 × V_{DDQ}:

$$MM_{PUPD} = \frac{R_{ON(PU)} - R_{ON(PD)}}{R_{ON,nom}} \times 100$$
 3. For IT and AT devices, the minimum values are derated by 6% when the device operates between -40°C and 0°C (T_C).
A larger maximum limit will result in slightly lower minimum currents.

DDR3L 40 Ohm Output Driver Sensitivity

If either the temperature or the voltage changes after I/O calibration, then the tolerance limits listed in Table 63 can be expected to widen according to Table 64 and Table 65 (page 75).

Table 64: DDR3L 40 Ohm Output Driver Sensitivity Definition

Symbol	Min	Max	Unit
R _{ON(PD)} @ 0.2 × V _{DDQ}	0.6 - dR _{ONdTL} × ΔT - dR _{ONdVL} × ΔV	1.1 + dR _{ONdTL} × ΔT + dR _{ONdVL} × ΔV	RZQ/6
R _{ON(PD)} @ 0.5 × V _{DDQ}	0.9 - dR _{ONdTM} × ΔT - dR _{ONdVM} × ΔV	1.1 + dR _{ONdTM} × ΔT + dR _{ONdVM} × ΔV	RZQ/6
R _{ON(PD)} @ 0.8 × V _{DDQ}	0.9 - dR _{ONdTH} × ΔT - dR _{ONdVH} × ΔV	1.4 + dR _{ONdTH} × ΔT + dR _{ONdVH} × ΔV	RZQ/6
R _{ON(PU)} @ 0.2 × V _{DDQ}	0.9 - dR _{ONdTL} × ΔT - dR _{ONdVL} × ΔV	1.4 + dR _{ONdTL} × ΔT + dR _{ONdVL} × ΔV	RZQ/6
R _{ON(PU)} @ 0.5 × V _{DDQ}	0.9 - dR _{ONdTM} × ΔT - dR _{ONdVM} × ΔV	1.1 + dR _{ONdTM} × ΔT + dR _{ONdVM} × ΔV	RZQ/6
R _{ON(PU)} @ 0.8 × V _{DDQ}	0.6 - dR _{ONdTH} × ΔT - dR _{ONdVH} × ΔV	1.1 + dR _{ONdTH} × ΔT + dR _{ONdVH} × ΔV	RZQ/6

Note: 1. ΔT = T - T_(@CALIBRATION); ΔV = V_{DDQ} - V_{DDQ(@CALIBRATION)}; and V_{DD} = V_{DDQ}.

Table 65: 40 Ohm Output Driver Voltage and Temperature Sensitivity

Change	Min	Max	Unit
dR _{ON} dTM	0	1.5	%/°C
dR _{ON} dVM	0	0.15	%/mV
dR _{ON} dTL	0	1.5	%/°C
dR _{ON} dVL	0	0.15	%/mV
dR _{ON} dTH	0	1.5	%/°C
dR _{ON} dVH	0	0.15	%/mV

Output Characteristics and Operating Conditions

Table 66: DDR3L Single-Ended Output Driver Characteristics

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output leakage current: DQ are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$; ODT is disabled; ODT is HIGH	I_{OZ}	-5	5	μA	1
Output slew rate: Single-ended; For rising and falling edges, measure between $V_{OL(AC)} = V_{REF} - 0.09 \times V_{DDQ}$ and $V_{OH(AC)} = V_{REF} + 0.09 \times V_{DDQ}$	SRQ_{se}	1.75	6	V/ns	1, 2, 3, 4
Single-ended DC high-level output voltage	$V_{OH(DC)}$	$0.8 \times V_{DDQ}$		V	1, 2, 5
Single-ended DC mid-point level output voltage	$V_{OM(DC)}$	$0.5 \times V_{DDQ}$		V	1, 2, 5
Single-ended DC low-level output voltage	$V_{OL(DC)}$	$0.2 \times V_{DDQ}$		V	1, 2, 5
Single-ended AC high-level output voltage	$V_{OH(AC)}$	$V_{TT} + 0.1 \times V_{DDQ}$		V	1, 2, 3, 6
Single-ended AC low-level output voltage	$V_{OL(AC)}$	$V_{TT} - 0.1 \times V_{DDQ}$		V	1, 2, 3, 6
Delta R_{ON} between pull-up and pull-down for DQ/DQS	MM_{PUPD}	-10	10	%	1, 7
Test load for AC timing and output slew rates	Output to V_{TT} ($V_{DDQ}/2$) via 25 Ω resistor				3

- Notes:
1. RZQ of 240 $\Omega \pm 1\%$ with RZQ/7 enabled (default 34 Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$; $V_{SSQ} = V_{SS}$).
 2. $V_{TT} = V_{DDQ}/2$.
 3. See Figure 27 (page 79) for the test load configuration.
 4. The 6 V/ns maximum is applicable for a single DQ signal when it is switching either from HIGH to LOW or LOW to HIGH while the remaining DQ signals in the same byte lane are either all static or all switching in the opposite direction. For all other DQ signal switching combinations, the maximum limit of 6 V/ns is reduced to 5 V/ns.
 5. See Figure 24 (page 70) for IV curve linearity. Do not use AC test load.
 6. See Table 69 (page 79) for output slew rate.
 7. See Figure 24 (page 70) for additional information.
 8. See Figure 25 (page 77) for an example of a single-ended output signal.

Figure 25: DQ Output Signal

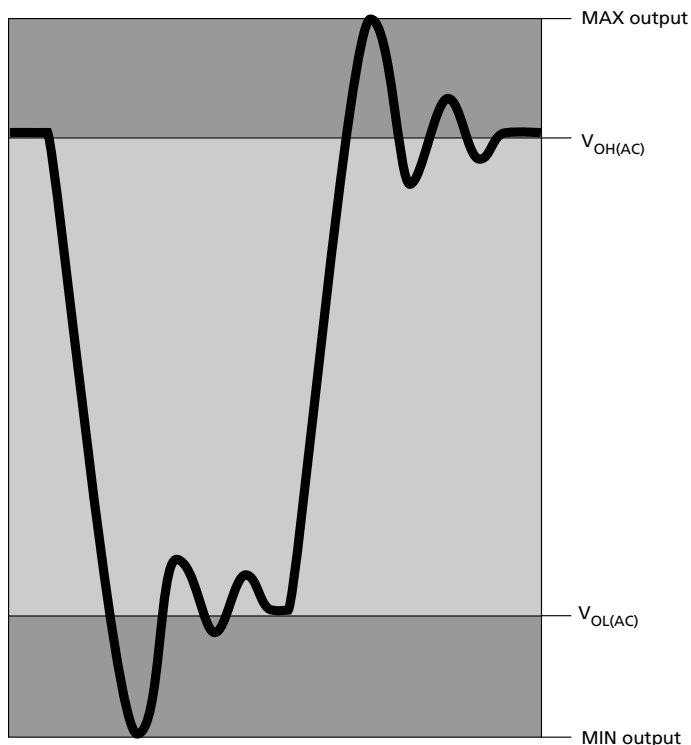


Table 67: DDR3L Differential Output Driver Characteristics

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output leakage current: DQ are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$; ODT is disabled; ODT is HIGH	I_{OZ}	-5	5	μA	1
DDR3L Output slew rate: Differential; For rising and falling edges, measure between $V_{OL,diff(AC)} = -0.18 \times V_{DDQ}$ and $V_{OH,diff(AC)} = 0.18 \times V_{DDQ}$	SRQ_{diff}	3.5	12	V/ns	1
Differential high-level output voltage	$V_{OH,diff(AC)}$	$+0.2 \times V_{DDQ}$		V	1, 4
Differential low-level output voltage	$V_{OL,diff(AC)}$	$-0.2 \times V_{DDQ}$		V	1, 4
Delta Ron between pull-up and pull-down for DQ/DQS	MM_{PUPD}	-10	10	%	1, 5
Test load for AC timing and output slew rates	Output to V_{TT} ($V_{DDQ}/2$) via 25 Ω resistor				3

- Notes:
1. RZQ of $240\Omega \pm 1\%$ with RZQ/7 enabled (default 34 Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$; $V_{SSQ} = V_{SS}$).
 2. $V_{REF} = V_{DDQ}/2$; slew rate @ 5 V/ns, interpolate for faster slew rate.
 3. See Figure 27 (page 79) for the test load configuration.
 4. See Table 70 (page 81) for the output slew rate.
 5. See Table 56 (page 71) for additional information.
 6. See Figure 26 (page 78) for an example of a differential output signal.

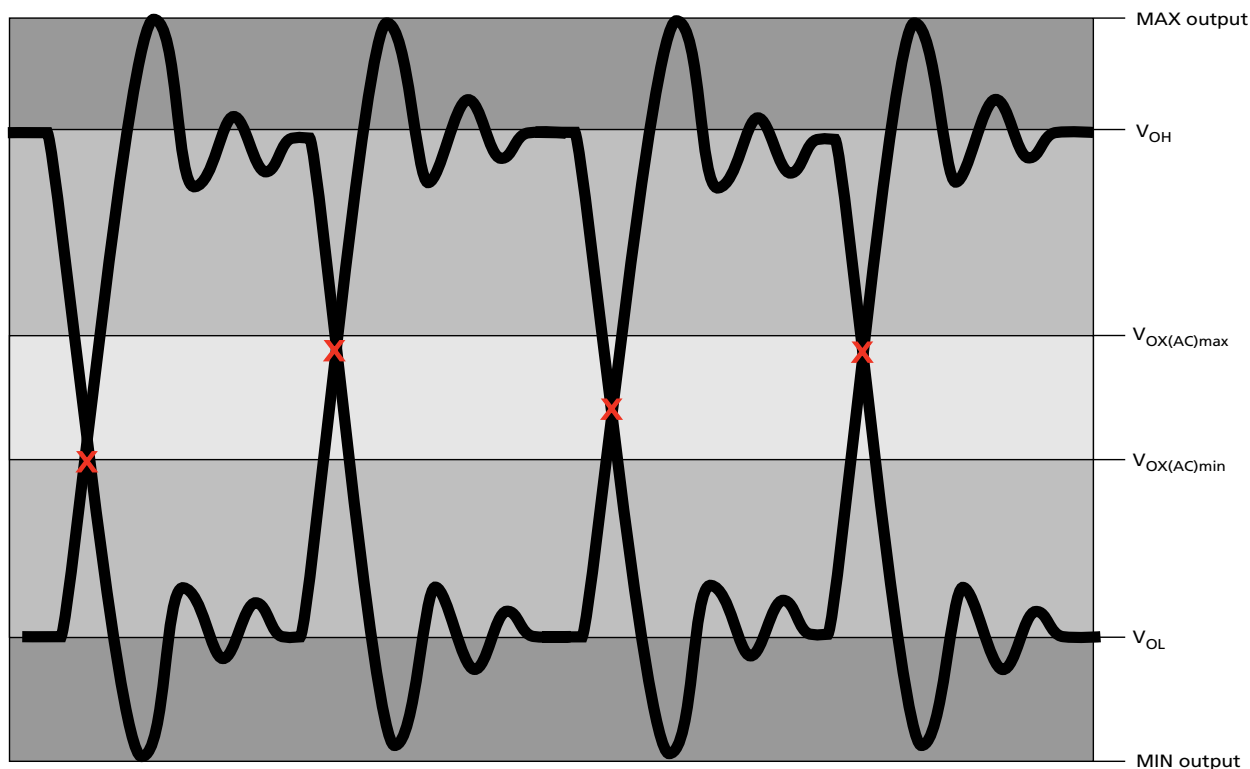
Table 68: DDR3L Differential Output Driver Characteristics $V_{OX(AC)}$

All voltages are referenced to V_{SS}

Parameter/Condition	Symbol		DDR3L- 800/1066/1333 DQS/DQS# Differential Slew Rate									Unit
			3.5V/ns	4V/ns	5V/ns	6V/ns	7V/ns	8V/ns	9V/ns	10V/ns	12V/ns	
Output differential crosspoint voltage	$V_{OX(AC)}$	Max	+115	+130	+135	+195	+205	+205	+205	+205	+205	mV
		Min	-115	-130	-135	-195	-205	-205	-205	-205	-205	mV
Parameter/Condition	Symbol		DDR3L-1600/1866 DQS/DQS# Differential Slew Rate									Unit
			3.5V/ns	4V/ns	5V/ns	6V/ns	7V/ns	8V/ns	9V/ns	10V/ns	12V/ns	
Output differential crosspoint voltage	$V_{OX(AC)}$	Max	+90	+105	+135	+155	+180	+205	+205	+205	+205	mV
		Min	-90	-105	-135	-155	-180	-205	-205	-205	-205	mV

- Notes:
1. RZQ of $240\Omega \pm 1\%$ with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage ($V_{DDQ} = V_{DD}$; $V_{SSQ} = V_{SS}$).
 2. See Figure 27 (page 79) for the test load configuration.
 3. See Figure 26 (page 78) for an example of a differential output signal.
 4. For a differential slew rate between the list values, the $V_{OX(AC)}$ value may be obtained by linear interpolation.

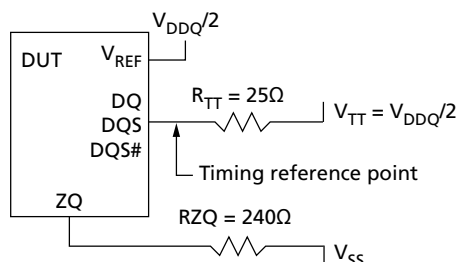
Figure 26: Differential Output Signal



Reference Output Load

Figure 27 represents the effective reference load of 25Ω used in defining the relevant device AC timing parameters (except ODT reference timing) as well as the output slew rate measurements. It is not intended to be a precise representation of a particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment.

Figure 27: Reference Output Load for AC Timing and Output Slew Rate



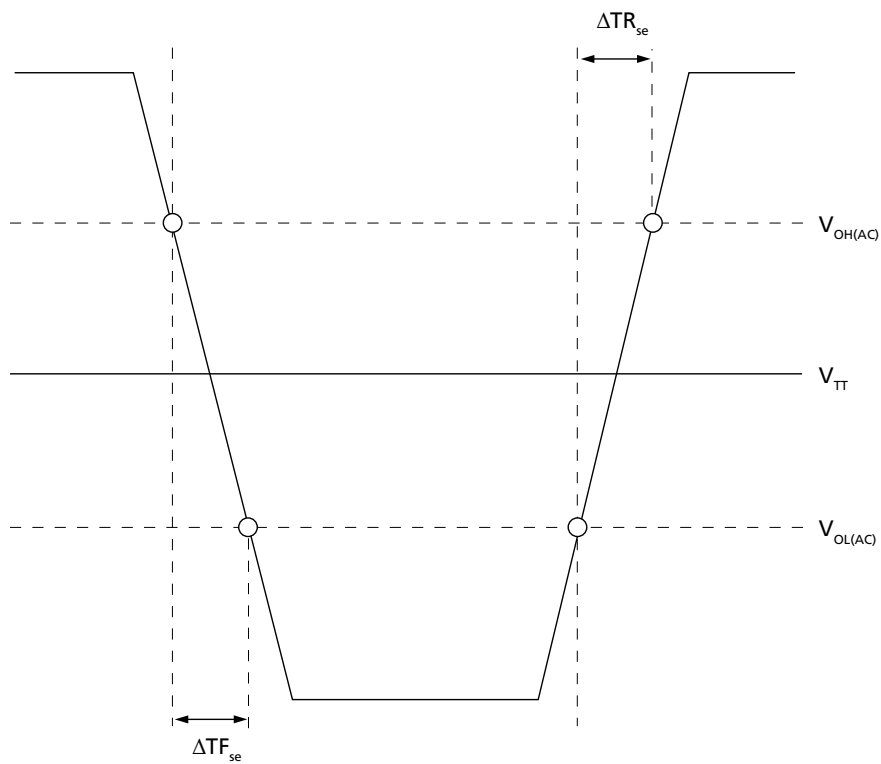
Slew Rate Definitions for Single-Ended Output Signals

The single-ended output driver is summarized in Table 66 (page 76). With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single-ended signals.

Table 69: Single-Ended Output Slew Rate Definition

Single-Ended Output Slew Rates (Linear Signals)		Measured		Calculation
Output	Edge	From	To	
DQ	Rising	$V_{OL(AC)}$	$V_{OH(AC)}$	$\frac{V_{OH(AC)} - V_{OL(AC)}}{\Delta T_{R_{se}}}$
	Falling	$V_{OH(AC)}$	$V_{OL(AC)}$	$\frac{V_{OH(AC)} - V_{OL(AC)}}{\Delta T_{F_{se}}}$

Figure 28: Nominal Slew Rate Definition for Single-Ended Output Signals



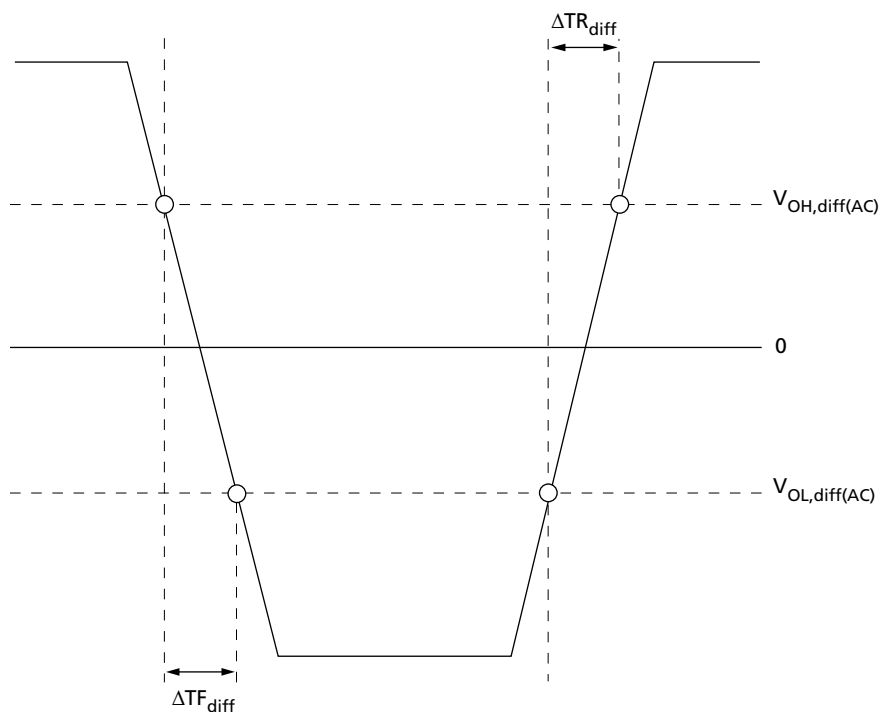
Slew Rate Definitions for Differential Output Signals

The differential output driver is summarized in Table 67 (page 77). With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for differential signals.

Table 70: Differential Output Slew Rate Definition

Differential Output Slew Rates (Linear Signals)		Measured		Calculation
Output	Edge	From	To	
DQS, DQS#	Rising	$V_{OL,diff(AC)}$	$V_{OH,diff(AC)}$	$\frac{V_{OH,diff(AC)} - V_{OL,diff(AC)}}{\Delta TR_{diff}}$
	Falling	$V_{OH,diff(AC)}$	$V_{OL,diff(AC)}$	$\frac{V_{OH,diff(AC)} - V_{OL,diff(AC)}}{\Delta TF_{diff}}$

Figure 29: Nominal Differential Output Slew Rate Definition for DQS, DQS#



Speed Bin Tables

Table 71: DDR3L-1066 Speed Bins

DDR3L-1066 Speed Bin			-187E		-187			
CL- ^t RCD- ^t RP			7-7-7		8-8-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes	
Internal READ command to first data	^t AA	13.125	–	15	–	ns		
ACTIVATE to internal READ or WRITE delay time	^t RCD	13.125	–	15	–	ns		
PRECHARGE command period	^t RP	13.125	–	15	–	ns		
ACTIVATE-to-ACTIVATE or REFRESH command period	^t RC	50.625	–	52.5	–	ns		
ACTIVATE-to-PRECHARGE command period	^t RAS	37.5	9 x ^t REFI	37.5	9 x ^t REFI	ns	1	
CL = 5	CWL = 5	^t CK (AVG)	3.0	3.3	3.0	3.3	ns	2
	CWL = 6	^t CK (AVG)	Reserved		Reserved		ns	3
CL = 6	CWL = 5	^t CK (AVG)	2.5	3.3	2.5	3.3	ns	2
	CWL = 6	^t CK (AVG)	Reserved		Reserved		ns	3
CL = 7	CWL = 5	^t CK (AVG)	Reserved		Reserved		ns	3
	CWL = 6	^t CK (AVG)	1.875	<2.5	Reserved		ns	2, 3
CL = 8	CWL = 5	^t CK (AVG)	Reserved		Reserved		ns	3
	CWL = 6	^t CK (AVG)	1.875	<2.5	1.875	<2.5	ns	2
Supported CL settings			5, 6, 7, 8		5, 6, 8		CK	
Supported CWL settings			5, 6		5, 6		CK	

- Notes:
- ^tREFI depends on T_{OPER}.
 - The CL and CWL settings result in ^tCK requirements. When making a selection of ^tCK, both CL and CWL requirement settings need to be fulfilled.
 - Reserved settings are not allowed.

Table 72: DDR3L-1333 Speed Bins

DDR3L-1333 Speed Bin			-15E ¹		-15 ²		Unit	Notes
CL- ^t RCD- ^t RP			9-9-9		10-10-10			
Parameter	Symbol		Min	Max	Min	Max		
Internal READ command to first data	^t AA		13.5	–	15	–	ns	
ACTIVATE to internal READ or WRITE delay time	^t RCD		13.5	–	15	–	ns	
PRECHARGE command period	^t RP		13.5	–	15	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period	^t RC		49.5	–	51	–	ns	
ACTIVATE-to-PRECHARGE command period	^t RAS		36	9 x ^t REFI	36	9 x ^t REFI	ns	3
CL = 5	CWL = 5	^t CK (AVG)	3.0	3.3	3.0	3.3	ns	4
	CWL = 6, 7	^t CK (AVG)	Reserved		Reserved		ns	5
CL = 6	CWL = 5	^t CK (AVG)	2.5	3.3	2.5	3.3	ns	4
	CWL = 6	^t CK (AVG)	Reserved		Reserved		ns	5
	CWL = 7	^t CK (AVG)	Reserved		Reserved		ns	5
CL = 7	CWL = 5	^t CK (AVG)	Reserved		Reserved		ns	5
	CWL = 6	^t CK (AVG)	1.875	<2.5	Reserved		ns	4, 5
	CWL = 7	^t CK (AVG)	Reserved		Reserved		ns	5
CL = 8	CWL = 5	^t CK (AVG)	Reserved		Reserved		ns	5
	CWL = 6	^t CK (AVG)	1.875	<2.5	1.875	<2.5	ns	4
	CWL = 7	^t CK (AVG)	Reserved		Reserved		ns	5
CL = 9	CWL = 5, 6	^t CK (AVG)	Reserved		Reserved		ns	5
	CWL = 7	^t CK (AVG)	1.5	<1.875	Reserved		ns	4, 5
CL = 10	CWL = 5, 6	^t CK (AVG)	Reserved		Reserved		ns	5
	CWL = 7	^t CK (AVG)	1.5	<1.875	1.5	<1.875	ns	4
Supported CL settings			5, 6, 7, 8, 9, 10		5, 6, 8, 10		CK	
Supported CWL settings			5, 6, 7		5, 6, 7		CK	

- Notes:
1. The -15E speed grade is backward compatible with 1066, CL = 7 (-187E).
 2. The -15 speed grade is backward compatible with 1066, CL = 8 (-187).
 3. ^tREFI depends on T_{OPER}.
 4. The CL and CWL settings result in ^tCK requirements. When making a selection of ^tCK, both CL and CWL requirement settings need to be fulfilled.
 5. Reserved settings are not allowed.

Table 73: DDR3L-1600 Speed Bins

DDR3L-1600 Speed Bin			-125 ¹			
CL- ^t RCD- ^t RP			11-11-11			
Parameter		Symbol	Min	Max	Unit	Notes
Internal READ command to first data		^t AA	13.75	–	ns	
ACTIVATE to internal READ or WRITE delay time		^t RCD	13.75	–	ns	
PRECHARGE command period		^t RP	13.75	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		^t RC	48.75	–	ns	
ACTIVATE-to-PRECHARGE command period		^t RAS	35	9 x ^t REFI	ns	2
CL = 5	CWL = 5	^t CK (AVG)	3.0	3.3	ns	3
	CWL = 6, 7, 8	^t CK (AVG)	Reserved		ns	4
CL = 6	CWL = 5	^t CK (AVG)	2.5	3.3	ns	3
	CWL = 6	^t CK (AVG)	Reserved		ns	4
	CWL = 7, 8	^t CK (AVG)	Reserved		ns	4
CL = 7	CWL = 5	^t CK (AVG)	Reserved		ns	4
	CWL = 6	^t CK (AVG)	1.875	<2.5	ns	3
	CWL = 7	^t CK (AVG)	Reserved		ns	4
	CWL = 8	^t CK (AVG)	Reserved		ns	4
CL = 8	CWL = 5	^t CK (AVG)	Reserved		ns	4
	CWL = 6	^t CK (AVG)	1.875	<2.5	ns	3
	CWL = 7	^t CK (AVG)	Reserved		ns	4
	CWL = 8	^t CK (AVG)	Reserved		ns	4
CL = 9	CWL = 5, 6	^t CK (AVG)	Reserved		ns	4
	CWL = 7	^t CK (AVG)	1.5	<1.875	ns	3
	CWL = 8	^t CK (AVG)	Reserved		ns	4
CL = 10	CWL = 5, 6	^t CK (AVG)	Reserved		ns	4
	CWL = 7	^t CK (AVG)	1.5	<1.875	ns	3
	CWL = 8	^t CK (AVG)	Reserved		ns	4
CL = 11	CWL = 5, 6, 7	^t CK (AVG)	Reserved		ns	4
	CWL = 8	^t CK (AVG)	1.25	<1.5	ns	3
Supported CL settings			5, 6, 7, 8, 9, 10, 11		CK	
Supported CWL settings			5, 6, 7, 8		CK	

- Notes:
1. The -125 speed grade is backward compatible with 1333, CL = 9 (-15E) and 1066, CL = 7 (-187E).
 2. ^tREFI depends on T_{OPER}.
 3. The CL and CWL settings result in ^tCK requirements. When making a selection of ^tCK, both CL and CWL requirement settings need to be fulfilled.
 4. Reserved settings are not allowed.

Table 74: DDR3L-1866 Speed Bins

DDR3L-1866 Speed Bin			-107 ¹		Unit	Notes
CL- ^t RCD- ^t RP			13-13-13			
Parameter		Symbol	Min	Max		
Internal READ command to first data		^t AA	13.91	20		
ACTIVATE to internal READ or WRITE delay time		^t RCD	13.91	–	ns	
PRECHARGE command period		^t RP	13.91	–	ns	
ACTIVATE-to-ACTIVATE or REFRESH command period		^t RC	47.91	–	ns	
ACTIVATE-to-PRECHARGE command period		^t RAS	34	9 x ^t REFI	ns	2
CL = 5	CWL = 5	^t CK (AVG)	3.0	3.3	ns	3
	CWL = 6, 7, 8, 9	^t CK (AVG)	Reserved		ns	4
CL = 6	CWL = 5	^t CK (AVG)	2.5	3.3	ns	3
	CWL = 6, 7, 8, 9	^t CK (AVG)	Reserved		ns	4
CL = 7	CWL = 5, 7, 8, 9	^t CK (AVG)	Reserved		ns	4
	CWL = 6	^t CK (AVG)	1.875	<2.5	ns	3
CL = 8	CWL = 5, 8, 9	^t CK (AVG)	Reserved		ns	4
	CWL = 6	^t CK (AVG)	1.875	<2.5	ns	3
	CWL = 7	^t CK (AVG)	Reserved		ns	4
CL = 9	CWL = 5, 6, 8, 9	^t CK (AVG)	Reserved		ns	4
	CWL = 7	^t CK (AVG)	1.5	<1.875	ns	3
CL = 10	CWL = 5, 6, 9	^t CK (AVG)	Reserved		ns	4
	CWL = 7	^t CK (AVG)	1.5	<1.875	ns	3
	CWL = 8	^t CK (AVG)	Reserved		ns	4
CL = 11	CWL = 5, 6, 7	^t CK (AVG)	Reserved		ns	4
	CWL = 8	^t CK (AVG)	1.25	<1.5	ns	3
	CWL = 9	^t CK (AVG)	Reserved		ns	4
CL = 12	CWL = 5, 6, 7, 8	^t CK (AVG)	Reserved		ns	4
	CWL = 9	^t CK (AVG)	Reserved		ns	4
CL = 13	CWL = 5, 6, 7, 8	^t CK (AVG)	Reserved		ns	4
	CWL = 9	^t CK (AVG)	1.07	<1.25	ns	3
Supported CL settings			5, 6, 7, 8, 9, 10, 11, 13		CK	
Supported CWL settings			5, 6, 7, 8, 9		CK	

- Notes:
1. The -107 speed grade is backward compatible with 1600, CL = 11 (-125) , 1333, CL = 9 (-15E) and 1066, CL = 7 (-187E).
 2. ^tREFI depends on T_{OPER}.
 3. The CL and CWL settings result in ^tCK requirements. When making a selection of ^tCK, both CL and CWL requirement settings need to be fulfilled.
 4. Reserved settings are not allowed.

Electrical Characteristics and AC Operating Conditions

Table 75: Electrical Characteristics and AC Operating Conditions

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L -800		DDR3L -1066		DDR3L -1333		DDR3L -1600		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing												
Clock period average: DLL dis- able mode	T _C ≤ 85°C	t _{CK} (DLL_DIS)	8	7800	8	7800	8	7800	8	7800	ns	9, 42
	T _C = >85°C to 95°C		8	3900	8	3900	8	3900	8	3900	ns	42
Clock period average: DLL enable mode		t _{CK} (AVG)	See Speed Bin Tables for t _{CK} range allowed								ns	10, 11
High pulse width average		t _{CH} (AVG)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	CK	12
Low pulse width average		t _{CL} (AVG)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	CK	12
Clock period jit- ter	DLL locked	t _{JITper}	−100	100	−90	90	−80	80	−70	70	ps	13
	DLL locking	t _{JITper,lck}	−90	90	−80	80	−70	70	−60	60	ps	13
Clock absolute period		t _{CK} (ABS)	MIN = t _{CK} (AVG) MIN + t _{JITper} MIN; MAX = t _{CK} (AVG) MAX + t _{JITper} MAX								ps	
Clock absolute high pulse width		t _{CH} (ABS)	0.43	–	0.43	–	0.43	–	0.43	–	t _{CK} (AVG)	14
Clock absolute low pulse width		t _{CL} (ABS)	0.43	–	0.43	–	0.43	–	0.43	–	t _{CK} (AVG)	15
Cycle-to-cycle jit- ter	DLL locked	t _{JITcc}	200		180		160		140		ps	16
	DLL locking	t _{JITcc,lck}	180		160		140		120		ps	16
Cumulative error across	2 cycles	t _{ERR2per}	−147	147	−132	132	−118	118	−103	103	ps	17
	3 cycles	t _{ERR3per}	−175	175	−157	157	−140	140	−122	122	ps	17
	4 cycles	t _{ERR4per}	−194	194	−175	175	−155	155	−136	136	ps	17
	5 cycles	t _{ERR5per}	−209	209	−188	188	−168	168	−147	147	ps	17
	6 cycles	t _{ERR6per}	−222	222	−200	200	−177	177	−155	155	ps	17
	7 cycles	t _{ERR7per}	−232	232	−209	209	−186	186	−163	163	ps	17
	8 cycles	t _{ERR8per}	−241	241	−217	217	−193	193	−169	169	ps	17
	9 cycles	t _{ERR9per}	−249	249	−224	224	−200	200	−175	175	ps	17
	10 cycles	t _{ERR10per}	−257	257	−231	231	−205	205	−180	180	ps	17
	11 cycles	t _{ERR11per}	−263	263	−237	237	−210	210	−184	184	ps	17
	12 cycles	t _{ERR12per}	−269	269	−242	242	−215	215	−188	188	ps	17
	n = 13, 14 . . . 49, 50 cycles	t _{ERRnper}	t _{ERRnper} MIN = (1 + 0.68ln[n]) × t _{JITper} MIN t _{ERRnper} MAX = (1 + 0.68ln[n]) × t _{JITper} MAX								ps	17
DQ Input Timing												
Data setup time to DQS, DQS#	Base (specifica- tion)	t _{DS} (AC160)	90	–	40	–	–	–	–	–	ps	18, 19, 44
	V _{REF} @ 1 V/ns		250	–	200	–	–	–	–	–	ps	19, 20

Table 75: Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L -800		DDR3L -1066		DDR3L -1333		DDR3L -1600		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Data setup time to DQS, DQS#	Base (specification)	t_{DS} (AC135)	140	–	90	–	45	–	25	–	ps	18, 19, 44
	V_{REF} @ 1 V/ns		275	–	250	–	180	–	160	–	ps	19, 20
Data hold time from DQS, DQS#	Base (specification)	t_{DH} (DC90)	160	–	110	–	75	–	55	–	ps	18, 19
	V_{REF} @ 1 V/ns		250	–	200	–	165	–	145	–	ps	19, 20
Minimum data pulse width		t_{DIPW}	600	–	490	–	400	–	360	–	ps	41
DQ Output Timing												
DQS, DQS# to DQ skew, per access		t_{DQSQ}	–	200	–	150	–	125	–	100	ps	
DQ output hold time from DQS, DQS#		t_{QH}	0.38	–	0.38	–	0.38	–	0.38	–	t_{CK} (AVG)	21
DQ Low-Z time from CK, CK#		t_{LZDQ}	–800	400	–600	300	–500	250	–450	225	ps	22, 23
DQ High-Z time from CK, CK#		t_{HZDQ}	–	400	–	300	–	250	–	225	ps	22, 23
DQ Strobe Input Timing												
DQS, DQS# rising to CK, CK# rising		t_{DQSS}	–0.25	0.25	–0.25	0.25	–0.25	0.25	–0.27	0.27	CK	25
DQS, DQS# differential input low pulse width		t_{DQSL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	CK	
DQS, DQS# differential input high pulse width		t_{DQSH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	CK	
DQS, DQS# falling setup to CK, CK# rising		t_{DSS}	0.2	–	0.2	–	0.2	–	0.18	–	CK	25
DQS, DQS# falling hold from CK, CK# rising		t_{DSH}	0.2	–	0.2	–	0.2	–	0.18	–	CK	25
DQS, DQS# differential WRITE preamble		t_{WPRE}	0.9	–	0.9	–	0.9	–	0.9	–	CK	
DQS, DQS# differential WRITE postamble		t_{WPST}	0.3	–	0.3	–	0.3	–	0.3	–	CK	
DQ Strobe Output Timing												
DQS, DQS# rising to/from rising CK, CK#		t_{DQSCK}	–400	400	–300	300	–255	255	–225	225	ps	23
DQS, DQS# rising to/from rising CK, CK# when DLL is disabled		t_{DQSCK} (DLL_DIS)	1	10	1	10	1	10	1	10	ns	26
DQS, DQS# differential output high time		t_{QSH}	0.38	–	0.38	–	0.40	–	0.40	–	CK	21
DQS, DQS# differential output low time		t_{QSL}	0.38	–	0.38	–	0.40	–	0.40	–	CK	21
DQS, DQS# Low-Z time (RL - 1)		t_{LZDQS}	–800	400	–600	300	–500	250	–450	225	ps	22, 23



2Gb: x4, x8, x16 DDR3L SDRAM Electrical Characteristics and AC Operating Conditions

Table 75: Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L -800		DDR3L -1066		DDR3L -1333		DDR3L -1600		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
DQS, DQS# High-Z time (RL + BL/2)		^t HZDQS	–	400	–	300	–	250	–	225	ps	22, 23
DQS, DQS# differential READ pre-amble		^t RPRE	0.9	Note 24	0.9	Note 24	0.9	Note 24	0.9	Note 24	CK	23, 24
DQS, DQS# differential READ postamble		^t RPST	0.3	Note 27	0.3	Note 27	0.3	Note 27	0.3	Note 27	CK	23, 27
Command and Address Timing												
DLL locking time		^t DLLK	512	–	512	–	512	–	512	–	CK	28
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	^t IS (AC160)	215	–	140	–	80	–	60	–	ps	29, 30, 44
	V _{REF} @ 1 V/ns		375	–	300	–	240	–	220	–	ps	20, 30
CTRL, CMD, ADDR setup to CK,CK#	Base (specification)	^t IS (AC135)	365	–	290	–	205	–	185	–	ps	29, 30, 44
	V _{REF} @ 1 V/ns		500	–	425	–	340	–	320	–	ps	20, 30
CTRL, CMD, ADDR hold from CK,CK#	Base (specification)	^t IH (DC90)	285	–	210	–	150	–	130	–	ps	29, 30
	V _{REF} @ 1 V/ns		375	–	300	–	240	–	220	–	ps	20, 30
Minimum CTRL, CMD, ADDR pulse width		^t IPW	900	–	780	–	620	–	560	–	ps	41
ACTIVATE to internal READ or WRITE delay		^t RCD	See Speed Bin Tables for ^t RCD								ns	31
PRECHARGE command period		^t RP	See Speed Bin Tables for ^t RP								ns	31
ACTIVATE-to-PRECHARGE command period		^t RAS	See Speed Bin Tables for ^t RAS								ns	31, 32
ACTIVATE-to-ACTIVATE command period		^t RC	See Speed Bin Tables for ^t RC								ns	31, 43
ACTIVATE-to-ACTIVATE minimum command period	x4/x8 (1KB page size)	^t RRD	MIN = greater of 4CK or 10ns		MIN = greater of 4CK or 7.5ns		MIN = greater of 4CK or 6ns		MIN = greater of 4CK or 6ns		CK	31
	x16 (2KB page size)		MIN = greater of 4CK or 10ns		MIN = greater of 4CK or 7.5ns		MIN = greater of 4CK or 7.5ns		CK	31		
Four ACTIVATE windows	x4/x8 (1KB page size)	^t FAW	40	–	37.5	–	30	–	30	–	ns	31
	x16 (2KB page size)		50	–	50	–	45	–	40	–	ns	31
Write recovery time		^t WR	MIN = 15ns; MAX = N/A								ns	31, 32, 33,34



2Gb: x4, x8, x16 DDR3L SDRAM

Electrical Characteristics and AC Operating Conditions

Table 75: Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L -800		DDR3L -1066		DDR3L -1333		DDR3L -1600		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Delay from start of internal WRITE transaction to internal READ command		^t WTR	MIN = greater of 4CK or 7.5ns; MAX = N/A								CK	31, 34
READ-to-PRECHARGE time		^t RTP	MIN = greater of 4CK or 7.5ns; MAX = N/A								CK	31, 32
CAS#-to-CAS# command delay		^t CCD	MIN = 4CK; MAX = N/A								CK	
Auto precharge write recovery + precharge time		^t DAL	MIN = WR + ^t RP/CK (AVG); MAX = N/A								CK	
MODE REGISTER SET command cycle time		^t MRD	MIN = 4CK; MAX = N/A								CK	
MODE REGISTER SET command update delay		^t MOD	MIN = greater of 12CK or 15ns; MAX = N/A								CK	
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		^t MPRR	MIN = 1CK; MAX = N/A								CK	
Calibration Timing												
ZQCL command: Long calibration time	POWER-UP and RESET operation	^t ZQinit	512	–	512	–	512	–	512	–	CK	
	Normal operation	^t ZQoper	256	–	256	–	256	–	256	–	CK	
ZQCS command: Short calibration time		^t ZQCS	64	–	64	–	64	–	64	–	CK	
Initialization and Reset Timing												
Exit reset from CKE HIGH to a valid command		^t XPR	MIN = greater of 5CK or ^t RFC + 10ns; MAX = N/A								CK	
Begin power supply ramp to power supplies stable		^t VDDPR	MIN = N/A; MAX = 200								ms	
RESET# LOW to power supplies stable		^t RPS	MIN = 0; MAX = 200								ms	
RESET# LOW to I/O and R _{TT} High-Z		^t IOZ	MIN = N/A; MAX = 20								ns	35
Refresh Timing												
REFRESH-to-ACTIVATE or REFRESH command period	^t RFC – 1Gb	MIN = 110; MAX = 70,200								ns		
	^t RFC – 2Gb	MIN = 160; MAX = 70,200								ns		
	^t RFC – 4Gb	MIN = 260; MAX = 70,200								ns		
	^t RFC – 8Gb	MIN = 350; MAX = 70,200								ns		

Table 75: Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L -800		DDR3L -1066		DDR3L -1333		DDR3L -1600		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Maximum refresh period	T _C ≤ 85°C	–	64 (1X)								ms	36
	T _C > 85°C		32 (2X)								ms	36
Maximum average periodic refresh	T _C ≤ 85°C	†REFI	7.8 (64ms/8192)								μs	36
	T _C > 85°C		3.9 (32ms/8192)								μs	36
Self Refresh Timing												
Exit self refresh to commands not requiring a locked DLL		†XS	MIN = greater of 5CK or †RFC + 10ns; MAX = N/A								CK	
Exit self refresh to commands requiring a locked DLL		†XSDLL	MIN = †DLLK (MIN); MAX = N/A								CK	28
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		†CKESR	MIN = †CKE (MIN) + CK; MAX = N/A								CK	
Valid clocks after self refresh entry or power-down entry		†CKSRE	MIN = greater of 5CK or 10ns; MAX = N/A								CK	
Valid clocks before self refresh exit, power-down exit, or reset exit		†CKSRX	MIN = greater of 5CK or 10ns; MAX = N/A								CK	
Power-Down Timing												
CKE MIN pulse width		†CKE (MIN)	Greater of 3CK or 7.5ns		Greater of 3CK or 5.625ns		Greater of 3CK or 5.625ns		Greater of 3CK or 5ns		CK	
Command pass disable delay		†CPDED	MIN = 1; MAX = N/A								CK	
Power-down entry to power-down exit timing		†PD	MIN = †CKE (MIN); MAX = 9 × †REFI								CK	
Begin power-down period prior to CKE registered HIGH		†ANPD	WL - 1CK								CK	
Power-down entry period: ODT either synchronous or asynchronous		PDE	Greater of †ANPD or †RFC - REFRESH command to CKE LOW time								CK	
Power-down exit period: ODT either synchronous or asynchronous		PDX	†ANPD + †XPDLL								CK	
Power-Down Entry Minimum Timing												
ACTIVATE command to power-down entry		†ACTPDEN	MIN = 1								CK	

Table 75: Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L -800		DDR3L -1066		DDR3L -1333		DDR3L -1600		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
PRECHARGE/PRECHARGE ALL command to power-down entry		t_{PRPDEN}	MIN = 1								CK	
REFRESH command to power-down entry		$t_{REFPDEN}$	MIN = 1								CK	37
MRS command to power-down entry		$t_{MRSPDEN}$	MIN = t_{MOD} (MIN)								CK	
READ/READ with auto precharge command to power-down entry		t_{RDPDEN}	MIN = $RL + 4 + 1$								CK	
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	t_{WRPDEN}	MIN = $WL + 4 + t_{WR}/t_{CK}$ (AVG)								CK	
	BC4MRS	t_{WRPDEN}	MIN = $WL + 2 + t_{WR}/t_{CK}$ (AVG)								CK	
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	$t_{WRAPDEN}$	MIN = $WL + 4 + WR + 1$								CK	
	BC4MRS	$t_{WRAPDEN}$	MIN = $WL + 2 + WR + 1$								CK	
Power-Down Exit Timing												
DLL on, any valid command, or DLL off to commands not requiring locked DLL		t_{XP}	MIN = greater of 3CK or 7.5ns; MAX = N/A				MIN = greater of 3CK or 6ns; MAX = N/A				CK	
Precharge power-down with DLL off to commands requiring a locked DLL		t_{XPDLL}	MIN = greater of 10CK or 24ns; MAX = N/A								CK	28
ODT Timing												
R_{TT} synchronous turn-on delay		ODTLon	CWL + AL - 2CK								CK	38
R_{TT} synchronous turn-off delay		ODTLoff	CWL + AL - 2CK								CK	40
R_{TT} turn-on from ODTL on reference		t_{AON}	-400	400	-300	300	-250	250	-225	225	ps	23, 38
R_{TT} turn-off from ODTL off reference		t_{AOF}	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	CK	39, 40
Asynchronous R_{TT} turn-on delay (power-down with DLL off)		t_{AONPD}	MIN = 2; MAX = 8.5								ns	38
Asynchronous R_{TT} turn-off delay (power-down with DLL off)		t_{AOFPD}	MIN = 2; MAX = 8.5								ns	40
ODT HIGH time with WRITE command and BL8		ODTH8	MIN = 6; MAX = N/A								CK	
ODT HIGH time without WRITE command or with WRITE command and BC4		ODTH4	MIN = 4; MAX = N/A								CK	

Table 75: Electrical Characteristics and AC Operating Conditions (Continued)

Notes 1–8 apply to the entire table

Parameter	Symbol	DDR3L -800		DDR3L -1066		DDR3L -1333		DDR3L -1600		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Dynamic ODT Timing											
R _{TT,nom} -to-R _{TT(WR)} change skew	ODTLcnw	WL - 2CK								CK	
R _{TT(WR)} -to-R _{TT,nom} change skew - BC4	ODTLcwn4	4CK + ODTLoff								CK	
R _{TT(WR)} -to-R _{TT,nom} change skew - BL8	ODTLcwn8	6CK + ODTLoff								CK	
R _{TT} dynamic change skew	t [‡] ADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	CK	39
Write Leveling Timing											
First DQS, DQS# rising edge	t [‡] WLMRD	40	–	40	–	40	–	40	–	CK	
DQS, DQS# delay	t [‡] WLDQSEN	25	–	25	–	25	–	25	–	CK	
Write leveling setup from rising CK, CK# crossing to rising DQS, DQS# crossing	t [‡] WLS	325	–	245	–	195	–	165	–	ps	
Write leveling hold from rising DQS, DQS# crossing to rising CK, CK# crossing	t [‡] WLH	325	–	245	–	195	–	165	–	ps	
Write leveling output delay	t [‡] WLO	0	9	0	9	0	9	0	7.5	ns	
Write leveling output error	t [‡] WLOE	0	2	0	2	0	2	0	2	ns	

- Notes:
1. AC timing parameters are valid from specified T_C MIN to T_C MAX values.
 2. All voltages are referenced to V_{SS} .
 3. Output timings are only valid for R_{ON34} output buffer selection.
 4. The unit t_{CK} (AVG) represents the actual t_{CK} (AVG) of the input clock under operation. The unit CK represents one clock cycle of the input clock, counting the actual clock edges.
 5. AC timing and I_{DD} tests may use a V_{IL} -to- V_{IH} swing of up to 900mV in the test environment, but input timing is still referenced to V_{REF} (except t_{IS} , t_{IH} , t_{DS} , and t_{DH} use the AC/DC trip points and CK, CK# and DQS, DQS# use their crossing points). The minimum slew rate for the input signals used to test the device is 1 V/ns for single-ended inputs and 2 V/ns for differential inputs in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
 6. All timings that use time-based values (ns, μ s, ms) should use t_{CK} (AVG) to determine the correct number of clocks (Table 75 (page 86) uses CK or t_{CK} [AVG] interchangeably). In the case of noninteger results, all minimum limits are to be rounded up to the nearest whole integer, and all maximum limits are to be rounded down to the nearest whole integer.
 7. Strobe or DQS_{diff} refers to the DQS and DQS# differential crossing point when DQS is the rising edge. Clock or CK refers to the CK and CK# differential crossing point when CK is the rising edge.
 8. This output load is used for all AC timing (except ODT reference timing) and slew rates. The actual test load may be different. The output signal voltage reference point is $V_{DDQ}/2$ for single-ended signals and the crossing point for differential signals (see Figure 26 (page 78)).

9. When operating in DLL disable mode, Micron does not warrant compliance with normal mode timings or functionality.
10. The clock's $t_{CK}^{(AVG)}$ is the average clock over any 200 consecutive clocks and $t_{CK}^{(AVG)}$ MIN is the smallest clock rate allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
11. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of $t_{CK}^{(AVG)}$ as a long-term jitter component; however, the spread spectrum may not use a clock rate below $t_{CK}^{(AVG)}$ MIN.
12. The clock's $t_{CH}^{(AVG)}$ and $t_{CL}^{(AVG)}$ are the average half clock period over any 200 consecutive clocks and is the smallest clock half period allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
13. The period jitter (t_{JITper}) is the maximum deviation in the clock period from the average or nominal clock. It is allowed in either the positive or negative direction.
14. $t_{CH}^{(ABS)}$ is the absolute instantaneous clock high pulse width as measured from one rising edge to the following falling edge.
15. $t_{CL}^{(ABS)}$ is the absolute instantaneous clock low pulse width as measured from one falling edge to the following rising edge.
16. The cycle-to-cycle jitter t_{JITcc} is the amount the clock period can deviate from one cycle to the next. It is important to keep cycle-to-cycle jitter at a minimum during the DLL locking time.
17. The cumulative jitter error $t_{ERRnper}$, where n is the number of clocks between 2 and 50, is the amount of clock time allowed to accumulate consecutively away from the average clock over n number of clock cycles.
18. $t_{DS}^{(base)}$ and $t_{DH}^{(base)}$ values are for a single-ended 1 V/ns slew rate DQs and 2 V/ns slew rate differential DQS, DQS#; when DQ single-ended slew rate is 2V/ns, the DQS differential slew rate is 4V/ns.
19. These parameters are measured from a data signal (DM, DQ0, DQ1, and so forth) transition edge to its respective data strobe signal (DQS, DQS#) crossing.
20. The setup and hold times are listed converting the base specification values (to which derating tables apply) to V_{REF} when the slew rate is 1 V/ns. These values, with a slew rate of 1 V/ns, are for reference only.
21. When the device is operated with input clock jitter, this parameter needs to be derated by the actual t_{JITper} (larger of $t_{JITper}^{(MIN)}$ or $t_{JITper}^{(MAX)}$ of the input clock (output deratings are relative to the SDRAM input clock).
22. Single-ended signal parameter.
23. The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present, even when within specification. This results in each parameter becoming larger. The following parameters are required to be derated by subtracting $t_{ERR10per}^{(MAX)}$: $t_{DQSCK}^{(MIN)}$, $t_{LZDQS}^{(MIN)}$, $t_{LZDQ}^{(MIN)}$, and $t_{AON}^{(MIN)}$. The following parameters are required to be derated by subtracting $t_{ERR10per}^{(MIN)}$: $t_{DQSCK}^{(MAX)}$, $t_{HZ}^{(MAX)}$, $t_{LZDQS}^{(MAX)}$, $t_{LZDQ}^{(MAX)}$, and $t_{AON}^{(MAX)}$. The parameter $t_{RPRE}^{(MIN)}$ is derated by subtracting $t_{JITper}^{(MAX)}$, while $t_{RPRE}^{(MAX)}$ is derated by subtracting $t_{JITper}^{(MIN)}$.
24. The maximum preamble is bound by $t_{LZDQS}^{(MAX)}$.
25. These parameters are measured from a data strobe signal (DQS, DQS#) crossing to its respective clock signal (CK, CK#) crossing. The specification values are not affected by the amount of clock jitter applied, as these are relative to the clock signal crossing. These parameters should be met whether clock jitter is present.
26. The $t_{DQSCK}^{(DLL_DIS)}$ parameter begins CL + AL - 1 cycles after the READ command.
27. The maximum postamble is bound by $t_{HZDQS}^{(MAX)}$.

28. Commands requiring a locked DLL are: READ (and RDAP) and synchronous ODT commands. In addition, after any change of latency t_{XPDLL} , timing must be met.
29. t_{IS} (base) and t_{IH} (base) values are for a single-ended 1 V/ns control/command/address slew rate and 2 V/ns CK, CK# differential slew rate.
30. These parameters are measured from a command/address signal transition edge to its respective clock (CK, CK#) signal crossing. The specification values are not affected by the amount of clock jitter applied as the setup and hold times are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present.
31. For these parameters, the DDR3 SDRAM device supports $t_{nPARAM}(nCK) = RU(t_{PARAM}[ns]/CK[AVG][ns])$, assuming all input clock jitter specifications are satisfied. For example, the device will support $t_{nRP}(nCK) = RU(t_{RP}/CK[AVG])$ if all input clock jitter specifications are met. This means that for DDR3-800 6-6-6, of which $t_{RP} = 5ns$, the device will support $t_{nRP} = RU(t_{RP}/CK[AVG]) = 6$ as long as the input clock jitter specifications are met. That is, the PRECHARGE command at T0 and the ACTIVATE command at T0 + 6 are valid even if six clocks are less than 15ns due to input clock jitter.
32. During READs and WRITEs with auto precharge, the DDR3 SDRAM will hold off the internal PRECHARGE command until $t_{RAS}(MIN)$ has been satisfied.
33. When operating in DLL disable mode, the greater of 4CK or 15ns is satisfied for t_{WR} .
34. The start of the write recovery time is defined as follows:
 - For BL8 (fixed by MRS or OTF): Rising clock edge four clock cycles after WL
 - For BC4 (OTF): Rising clock edge four clock cycles after WL
 - For BC4 (fixed by MRS): Rising clock edge two clock cycles after WL
35. RESET# should be LOW as soon as power starts to ramp to ensure the outputs are in High-Z. Until RESET# is LOW, the outputs are at risk of driving and could result in excessive current, depending on bus activity.
36. The refresh period is 64ms when T_C is less than or equal to 85°C. This equates to an average refresh rate of 7.8125μs. However, nine REFRESH commands should be asserted at least once every 70.3μs. When T_C is greater than 85°C, the refresh period is 32ms.
37. Although CKE is allowed to be registered LOW after a REFRESH command when $t_{REFPDEN}(MIN)$ is satisfied, there are cases where additional time such as $t_{XPDLL}(MIN)$ is required.
38. ODT turn-on time MIN is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time maximum is when the ODT resistance is fully on. The ODT reference load is shown in Figure 20 (page 67). Designs that were created prior to JEDEC tightening the maximum limit from 9ns to 8.5ns will be allowed to have a 9ns maximum.
39. Half-clock output parameters must be derated by the actual $t_{ERR10per}$ and t_{JITdy} when input clock jitter is present. This results in each parameter becoming larger. The parameters $t_{ADC}(MIN)$ and $t_{AOF}(MIN)$ are each required to be derated by subtracting both $t_{ERR10per}(MAX)$ and $t_{JITdy}(MAX)$. The parameters $t_{ADC}(MAX)$ and $t_{AOF}(MAX)$ are required to be derated by subtracting both $t_{ERR10per}(MAX)$ and $t_{JITdy}(MAX)$.
40. ODT turn-off time minimum is when the device starts to turn off ODT resistance. ODT turn-off time maximum is when the DRAM buffer is in High-Z. The ODT reference load is shown in Figure 20 (page 67). This output load is used for ODT timings (see Figure 27 (page 79)).
41. Pulse width of a input signal is defined as the width between the first crossing of $V_{REF(DC)}$ and the consecutive crossing of $V_{REF(DC)}$.
42. Should the clock rate be larger than $t_{RFC}(MIN)$, an AUTO REFRESH command should have at least one NOP command between it and another AUTO REFRESH command. Additionally, if the clock rate is slower than 40ns (25 MHz), all REFRESH commands should be followed by a PRECHARGE ALL command.

43. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in a reduction of REFRESH characteristics or product lifetime.
44. When two $V_{IH(AC)}$ values (and two corresponding $V_{IL(AC)}$ values) are listed for a specific speed bin, the user may choose either value for the input AC level. Whichever value is used, the associated setup time for that AC level must also be used. Additionally, one $V_{IH(AC)}$ value may be used for address/command inputs and the other $V_{IH(AC)}$ value may be used for data inputs.

For example, for DDR3-800, two input AC levels are defined: $V_{IH(AC175),min}$ and $V_{IH(AC150),min}$ (corresponding $V_{IL(AC175),min}$ and $V_{IL(AC150),min}$). For DDR3-800, the address/command inputs must use either $V_{IH(AC175),min}$ with $t_{IS(AC175)}$ of 200ps or $V_{IH(AC150),min}$ with $t_{IS(AC150)}$ of 350ps; independently, the data inputs must use either $V_{IH(AC175),min}$ with $t_{DS(AC175)}$ of 75ps or $V_{IH(AC150),min}$ with $t_{DS(AC150)}$ of 125ps.

Table 76: Electrical Characteristics and AC Operating Conditions for Speed Extensions

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1866		Unit	Notes
			Min	Max		
Clock Timing						
Clock period average: DLL disable mode	T _C = 0°C to 85°C	t ^{CK} (DLL_DIS)	8	7800	ns	9, 42
	T _C = >85°C to 95°C		8	3900	ns	42
Clock period average: DLL enable mode		t ^{CK} (AVG)	See Speed Bin Tables for t ^{CK} range allowed		ns	10, 11
High pulse width average		t ^{CH} (AVG)	0.47	0.53	CK	12
Low pulse width average		t ^{CL} (AVG)	0.47	0.53	CK	12
Clock period jitter	DLL locked	t ^{JITper}	–60	60	ps	13
	DLL locking	t ^{JITper,lck}	–50	50	ps	13
Clock absolute period		t ^{CK} (ABS)	MIN = t ^{CK} (AVG) MIN + t ^{JITper} MIN; MAX = t ^{CK} (AVG) MAX + t ^{JITper} MAX		ps	
Clock absolute high pulse width		t ^{CH} (ABS)	0.43	–	t ^{CK} (AVG)	14
Clock absolute low pulse width		t ^{CL} (ABS)	0.43	–	t ^{CK} (AVG)	15
Cycle-to-cycle jitter	DLL locked	t ^{JITcc}	120		ps	16
	DLL locking	t ^{JITcc,lck}	100		ps	16
Cumulative error across	2 cycles	t ^{ERR2per}	–88	88	ps	17
	3 cycles	t ^{ERR3per}	–105	105	ps	17
	4 cycles	t ^{ERR4per}	–117	117	ps	17
	5 cycles	t ^{ERR5per}	–126	126	ps	17
	6 cycles	t ^{ERR6per}	–133	133	ps	17
	7 cycles	t ^{ERR7per}	–139	139	ps	17
	8 cycles	t ^{ERR8per}	–145	145	ps	17
	9 cycles	t ^{ERR9per}	–150	150	ps	17
	10 cycles	t ^{ERR10per}	–154	154	ps	17
	11 cycles	t ^{ERR11per}	–158	158	ps	17
	12 cycles	t ^{ERR12per}	–161	161	ps	17
	n = 13, 14 . . . 49, 50 cycles	t ^{ERRnper}	t ^{ERRnper} MIN = (1 + 0.68ln[n]) × t ^{JITper} MIN t ^{ERRnper} MAX = (1 + 0.68ln[n]) × t ^{JITper} MAX		ps	17
DQ Input Timing						
Data setup time to DQS, DQS#	Base (specification) @ 2 V/ns	t ^{DS} (AC130)	70	–	ps	18, 19
	V _{REF} @ 2 V/ns		135	–	ps	19, 20

Table 76: Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1866		Unit	Notes
			Min	Max		
Data hold time from DQS, DQS#	Base (specification) @ 2 V/ns	t_{DH} (DC90)	75	–	ps	18, 19
	V_{REF} @ 2 V/ns		110	–	ps	19, 20
Minimum data pulse width		t_{DIPW}	320	–	ps	41
DQ Output Timing						
DQS, DQS# to DQ skew, per access		t_{DQSQ}	–	85	ps	
DQ output hold time from DQS, DQS#		t_{QH}	0.38	–	t_{CK} (AVG)	21
DQ Low-Z time from CK, CK#		t_{LZDQ}	–390	195	ps	22, 23
DQ High-Z time from CK, CK#		t_{HZDQ}	–	195	ps	22, 23
DQ Strobe Input Timing						
DQS, DQS# rising to CK, CK# rising		t_{DQSS}	–0.27	0.27	CK	25
DQS, DQS# differential input low pulse width		t_{DQSL}	0.45	0.55	CK	
DQS, DQS# differential input high pulse width		t_{DQSH}	0.45	0.55	CK	
DQS, DQS# falling setup to CK, CK# rising		t_{DSS}	0.18	–	CK	25
DQS, DQS# falling hold from CK, CK# rising		t_{DSH}	0.18	–	CK	25
DQS, DQS# differential WRITE preamble		t_{WPRE}	0.9	–	CK	
DQS, DQS# differential WRITE postamble		t_{WPST}	0.3	–	CK	
DQ Strobe Output Timing						
DQS, DQS# rising to/from rising CK, CK#		t_{DQSCK}	–195	195	ps	23
DQS, DQS# rising to/from rising CK, CK# when DLL is disabled		t_{DQSCK} (DLL_DIS)	1	10	ns	26
DQS, DQS# differential output high time		t_{QSH}	0.40	–	CK	21
DQS, DQS# differential output low time		t_{QSL}	0.40	–	CK	21
DQS, DQS# Low-Z time (RL - 1)		t_{LZDQS}	–390	195	ps	22, 23
DQS, DQS# High-Z time (RL + BL/2)		t_{HZDQS}	–	195	ps	22, 23
DQS, DQS# differential READ preamble		t_{RPRE}	0.9	Note 24	CK	23, 24
DQS, DQS# differential READ postamble		t_{RPST}	0.3	Note 27	CK	23, 27
Command and Address Timing						
DLL locking time		t_{DLLK}	512	–	CK	28
CTRL, CMD, ADDR setup to CK, CK#	Base (specification)	t_{IS} (AC135)	65	–	ps	29, 30, 44
	V_{REF} @ 1 V/ns		200	–	ps	20, 30
CTRL, CMD, ADDR setup to CK, CK#	Base (specification)	t_{IS} (AC125)	150	–	ps	29, 30, 44
	V_{REF} @ 1 V/ns		275	–	ps	20, 30
CTRL, CMD, ADDR hold from CK, CK#	Base (specification)	t_{IH} (DC90)	110	–	ps	29, 30
	V_{REF} @ 1 V/ns		200	–	ps	20, 30
Minimum CTRL, CMD, ADDR pulse width		t_{IPW}	535	–	ps	41

Table 76: Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1866		Unit	Notes
			Min	Max		
ACTIVATE to internal READ or WRITE delay		t_{RCD}	See Speed Bin Tables for t_{RCD}		ns	31
PRECHARGE command period		t_{RP}	See Speed Bin Tables for t_{RP}		ns	31
ACTIVATE-to-PRECHARGE command period		t_{RAS}	See Speed Bin Tables for t_{RAS}		ns	31, 32
ACTIVATE-to-ACTIVATE command period		t_{RC}	See Speed Bin Tables for t_{RC}		ns	31, 43
ACTIVATE-to-ACTIVATE minimum command period	1KB page size	t_{RRD}	MIN = greater of 4CK or 5ns		CK	31
	2KB page size		MIN = greater of 4CK or 6ns		CK	31
Four ACTIVATE windows	1KB page size	t_{FAW}	27	–	ns	31
	2KB page size		35	–	ns	31
Write recovery time		t_{WR}	MIN = 15ns; MAX = N/A		ns	31, 32, 33
Delay from start of internal WRITE transaction to internal READ command		t_{WTR}	MIN = greater of 4CK or 7.5ns; MAX = N/A		CK	31, 34
READ-to-PRECHARGE time		t_{RTP}	MIN = greater of 4CK or 7.5ns; MAX = N/A		CK	31, 32
CAS#-to-CAS# command delay		t_{CCD}	MIN = 4CK; MAX = N/A		CK	
Auto precharge write recovery + precharge time		t_{DAL}	MIN = WR + t_{RP}/t_{CK} (AVG); MAX = N/A		CK	
MODE REGISTER SET command cycle time		t_{MRD}	MIN = 4CK; MAX = N/A		CK	
MODE REGISTER SET command update delay		t_{MOD}	MIN = greater of 12CK or 15ns; MAX = N/A		CK	
MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit		t_{MPRR}	MIN = 1CK; MAX = N/A		CK	
Calibration Timing						
ZQCL command: Long calibration time	POWER-UP and RE-SET operation	t_{ZQinit}	MIN = N/A MAX = MAX(512nCK, 640ns)		CK	
	Normal operation	t_{ZQoper}	MIN = N/A MAX = MAX(256nCK, 320ns)		CK	
ZQCS command: Short calibration time			MIN = N/A MAX = MAX(64nCK, 80ns) t_{ZQCS}		CK	
Initialization and Reset Timing						
Exit reset from CKE HIGH to a valid command		t_{XPR}	MIN = greater of 5CK or t_{RFC} + 10ns; MAX = N/A		CK	

Table 76: Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1866		Unit	Notes
			Min	Max		
Begin power supply ramp to power supplies stable		tVDDPR	MIN = N/A; MAX = 200		ms	
RESET# LOW to power supplies stable		tRPS	MIN = 0; MAX = 200		ms	
RESET# LOW to I/O and R _{TT} High-Z		tIOZ	MIN = N/A; MAX = 20		ns	35
Refresh Timing						
REFRESH-to-ACTIVATE or REFRESH command period		tRFC – 1Gb	MIN = 110; MAX = 70,200		ns	
		tRFC – 2Gb	MIN = 160; MAX = 70,200		ns	
		tRFC – 4Gb	MIN = 260; MAX = 70,200		ns	
		tRFC – 8Gb	MIN = 350; MAX = 70,200		ns	
Maximum refresh period	T _C ≤ 85°C	–	64 (1X)		ms	36
	T _C > 85°C		32 (2X)		ms	36
Maximum average periodic refresh	T _C ≤ 85°C	tREFI	7.8 (64ms/8192)		µs	36
	T _C > 85°C		3.9 (32ms/8192)		µs	36
Self Refresh Timing						
Exit self refresh to commands not requiring a locked DLL		tXS	MIN = greater of 5CK or tRFC + 10ns; MAX = N/A		CK	
Exit self refresh to commands requiring a locked DLL		tXSDLL	MIN = tDLLK (MIN); MAX = N/A		CK	28
Minimum CKE low pulse width for self refresh entry to self refresh exit timing		tCKESR	MIN = tCKE (MIN) + CK; MAX = N/A		CK	
Valid clocks after self refresh entry or power-down entry		tCKSRE	MIN = greater of 5CK or 10ns; MAX = N/A		CK	
Valid clocks before self refresh exit, power-down exit, or reset exit		tCKSRX	MIN = greater of 5CK or 10ns; MAX = N/A		CK	
Power-Down Timing						
CKE MIN pulse width		tCKE (MIN)	Greater of 3CK or 5ns		CK	
Command pass disable delay		tCPDED	MIN = 2; MAX = N/A		CK	
Power-down entry to power-down exit timing		tPD	MIN = tCKE (MIN); MAX = 9 × tREFI		CK	
Begin power-down period prior to CKE registered HIGH		tANPD	WL - 1CK		CK	
Power-down entry period: ODT either synchronous or asynchronous		PDE	Greater of tANPD or tRFC - REFRESH command to CKE LOW time		CK	
Power-down exit period: ODT either synchronous or asynchronous		PDX	tANPD + tXPDLL		CK	
Power-Down Entry Minimum Timing						
ACTIVATE command to power-down entry		tACTPDEN	MIN = 2		CK	

Table 76: Electrical Characteristics and AC Operating Conditions for Speed Extensions (Continued)

Notes 1–8 apply to the entire table

Parameter		Symbol	DDR3L-1866		Unit	Notes
			Min	Max		
PRECHARGE/PRECHARGE ALL command to power-down entry		t_{PRPDEN}	MIN = 2		CK	
REFRESH command to power-down entry		$t_{REFPDEN}$	MIN = 2		CK	37
MRS command to power-down entry		$t_{MRSPDEN}$	MIN = t_{MOD} (MIN)		CK	
READ/READ with auto precharge command to power-down entry		t_{RDPDEN}	MIN = $RL + 4 + 1$		CK	
WRITE command to power-down entry	BL8 (OTF, MRS) BC4OTF	t_{WRPDEN}	MIN = $WL + 4 + t_{WR}/t_{CK}$ (AVG)		CK	
	BC4MRS	t_{WRPDEN}	MIN = $WL + 2 + t_{WR}/t_{CK}$ (AVG)		CK	
WRITE with auto precharge command to power-down entry	BL8 (OTF, MRS) BC4OTF	$t_{WRAPDEN}$	MIN = $WL + 4 + WR + 1$		CK	
	BC4MRS	$t_{WRAPDEN}$	MIN = $WL + 2 + WR + 1$		CK	
Power-Down Exit Timing						
DLL on, any valid command, or DLL off to commands not requiring locked DLL		t_{XP}	MIN = greater of 3CK or 6ns; MAX = N/A		CK	
Precharge power-down with DLL off to commands requiring a locked DLL		t_{XPDLL}	MIN = greater of 10CK or 24ns; MAX = N/A		CK	28
ODT Timing						
R_{TT} synchronous turn-on delay		ODTL on	CWL + AL - 2CK		CK	38
R_{TT} synchronous turn-off delay		ODTL off	CWL + AL - 2CK		CK	40
R_{TT} turn-on from ODTL on reference		t_{AON}	-195	195	ps	23, 38
R_{TT} turn-off from ODTL off reference		t_{AOF}	0.3	0.7	CK	39, 40
Asynchronous R_{TT} turn-on delay (power-down with DLL off)		t_{AONPD}	MIN = 2; MAX = 8.5		ns	38
Asynchronous R_{TT} turn-off delay (power-down with DLL off)		t_{AOFPD}	MIN = 2; MAX = 8.5		ns	40
ODT HIGH time with WRITE command and BL8		ODTH8	MIN = 6; MAX = N/A		CK	
ODT HIGH time without WRITE command or with WRITE command and BC4		ODTH4	MIN = 4; MAX = N/A		CK	
Dynamic ODT Timing						
$R_{TT,nom}$ -to- $R_{TT(WR)}$ change skew		ODTLcnw	WL - 2CK		CK	
$R_{TT(WR)}$ -to- $R_{TT,nom}$ change skew - BC4		ODTLcwn4	4CK + ODTLoff		CK	
$R_{TT(WR)}$ -to- $R_{TT,nom}$ change skew - BL8		ODTLcwn8	6CK + ODTLoff		CK	
R_{TT} dynamic change skew		t_{ADC}	0.3	0.7	CK	39
Write Leveling Timing						
First DQS, DQS# rising edge		t_{WLMRD}	40	–	CK	
DQS, DQS# delay		$t_{WLDQSEN}$	25	–	CK	