MP2760

I²C-Controlled, 1-Cell to 4-Cell Buck-Boost Charger with NVDC Power Path Management

DESCRIPTION

The MP2760 is a buck-boost charger for battery packs with 1 to 4 cells in series. It accepts a wide 4V to 22V input voltage (V_{IN}) range to charge the battery. The battery voltage can be above or below V_{IN} due to the buck-boost topology.

When the input is present, the MP2760 operates in charge mode. The device measures the battery voltage and charges the battery with four phases: constant current trickle charge, constant current pre-charge, constant current fast charge, and constant voltage charge. Additional features include charge termination and automatic recharge.

The MP2760 integrates the input current (I_{IN}) limit and V_{IN} limit to avoid overloading the input power source. This is compliant with USB PD specifications.

The MP2760 provides narrow-voltage DC (NVDC) power path management. A battery FET (BATFET) controls an external N-channel MOSFET to regulate the system's minimum voltage and provide a battery supplement function. The device can also supply a wide 4V to 21V voltage range at the IN pin when source mode is enabled. The MP2760 also has an IN output current in source mode (I_{IN_SRC}) limit up to 6A. These are compliant with USB PD specifications.

The charge and discharge parameters (e.g. I_{IN} limit, V_{IN} limit, charging current, battery full regulation voltage, IN output voltage in source mode (V_{IN_SRC}), and I_{IN_SRC}) can be configured via the I²C/SMBus interface. The MP2760 can also provide statuses and fault information through the I²C/SMBus registers.

To guarantee safe operation, the IC limits the die temperature to a configurable threshold. Other safety features include input over-voltage protection (OVP), battery OVP, system OVP, thermal shutdown, and a configurable timer to prevent prolonged charging of a dead battery.

The MP2760 is available in a TQFN-30 (4mmx5mm) package.

FEATURES

- Buck-Boost Charger for 1 to 4 Cells in Series Battery Pack
- 4V to 22V Input Voltage (V_{IN})
- Up to 26V Sustainable Voltage (Up to 28V with External MOSFET)
- Supports USB 2.0, USB 3.0, USB 3.1, USB 3.2, Type-C and USB PD 3.0 Settings
- Smooth Transition for Buck and Boost Mode
- Configurable Maximum Input Current (I_{IN}) Limit and Minimum V_{IN} Limit
- Up to 6A Configurable Charge Current
- Configurable Battery-Full Voltage Up to 4.68V/Cell with 0.5% Accuracy
- Configurable 4V to 21V IN Output Voltage in Source Mode (V_{IN_SRC}) with 20mV/Step
- Compatible with USB PD 3.0
- Up to 6A Output Current with 50mA/Step
- 500kHz to 1.2MHz Configurable f_{SW}
- I²C or SMBus Host Control Interface
- Input Power Source Status Indication Pin
- Integrated 10-Bit ADC for Monitoring
- Analog Output Pin to Monitor Battery Current in Charge Mode and Source Mode
- Input OVP, System OVP, and Battery OVP
- System SCP in Charge Mode
- Output SCP in USB PD Source Mode
- Battery Missing Detection
- NTC Pin Floating Detection
- Integrated N-Channel MOSFET for Input Power Pass-Through or OVP
- Integrated N-Channel MOSFET for NVDC Power Path Control
- Configurable Battery Temperature Protection Threshold, Compliant with JEITA
- Thermal Regulation and Thermal Shutdown
- Available in a TQFN-30 (4mmx5mm) Package

APPLICATIONS

- Ultrabooks, Notebooks, Tablets
- USB PD Devices
- General Multiple-Cell Applications

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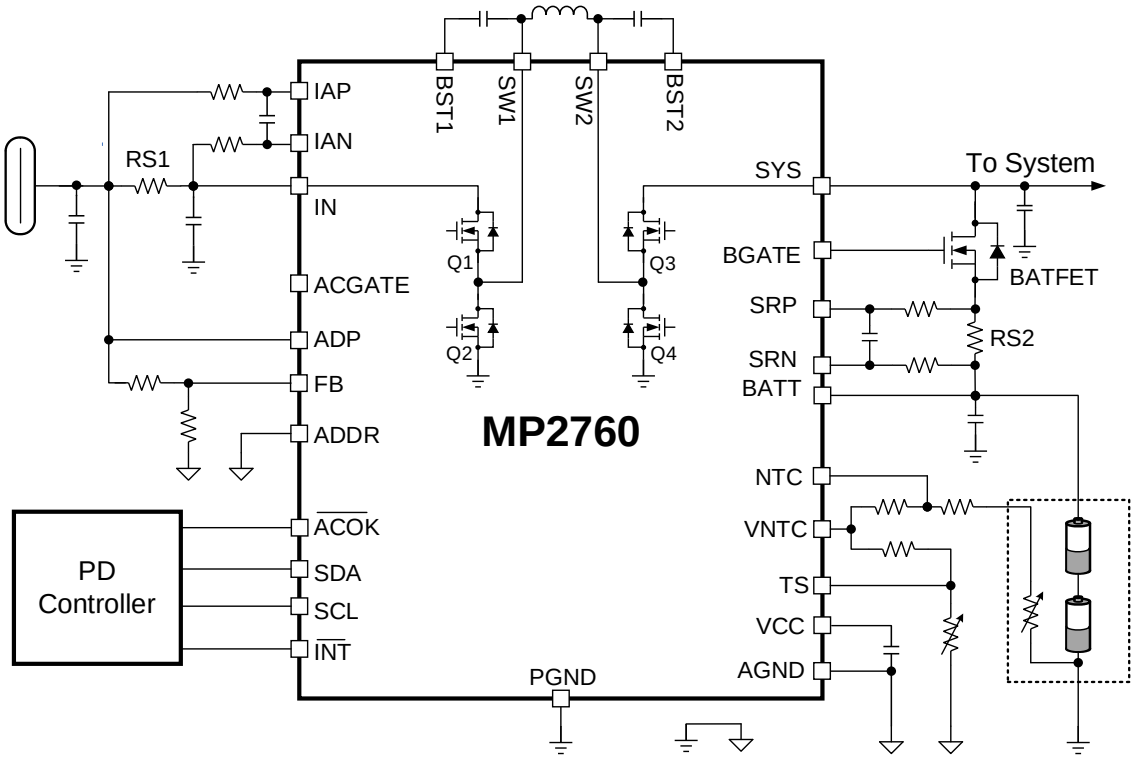
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2760GVT-xxxx**	TQFN-30 (4mmx5mm)	*See Below*	1
MP2760GVT-000A***		*See Below*	1
MP2760GVT-010A****		*See Below*	1
MP2760GVT-030A*****		*See Below*	1
MP2760GVT-040A******		*See Below*	1
EVKT-MP2760	Evaluation kit	*See Below*	-

* For Tape & Reel, add suffix -Z (e.g. MP2760GVT-xxxx-Z).

** "xxxx" is the register setting option. Contact an MPS FAE to obtain an "xxxx" value.

*** "-000A" is the factory default for 2-cell applications. This content can be viewed in the I²C register map.

**** "-010A" is the factory default for 1-cell applications.

***** "-030A" is the factory default for 3-cell applications.

****** "-040A" is the factory default for 4-cell applications.

TOP MARKING

MPSYWW

MP2760

LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP2760: Part number
LLLLLL: Lot number

EVALUATION KIT EVKT-MP2760

EVKT-MP2760 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2760-VT-00A	MP2760 evaluation board	1
2	EVKT-USBI2C-02 bag	Includes one USB to I²C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

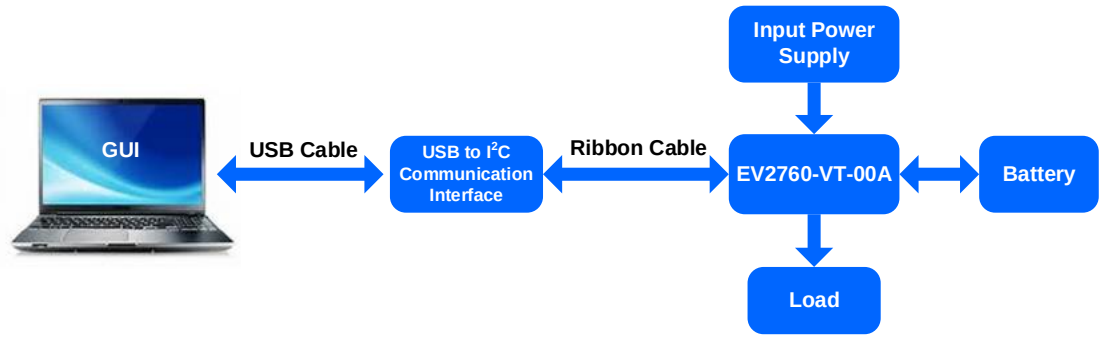

Figure 1: EVKT-MP2760 Evaluation Kit Set-Up

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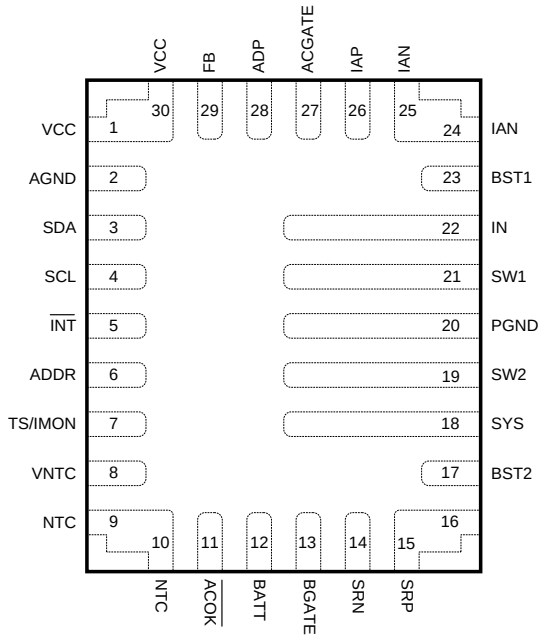
PACKAGE REFERENCE

TOP VIEW



TQFN-30 (4mmx5mm)

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PIN FUNCTIONS

Pin #	Name	Description
1, 30	VCC	**VCC LDO output.** Connect a 4.7μF ceramic capacitor from the VCC pin to AGND. VCC is a 3.6V output that can pull up the internal circuit and open-drain pins.
2	AGND	**Analog ground.** All parameter settings refer to this ground.
3	SDA	**I²C/SMBus data.** The SDA pin is an open drain. Connect SDA to the logic rail through a 10kΩ resistor.
4	SCL	**I²C/SMBus clock.** The SCL pin is an open drain. Connect SCL to the logic rail through a 10kΩ resistor.
5	$\overline{\text{INT}}$	**Interrupt request output.** This pin is open-drain structure that must be pulled up to VCC via an external 10kΩ resistor.
6	ADDR	**Internal use.** Connect a resistor less than 115kΩ to the AGND pin.
7	TS/IMON	**Temperature sense/current monitoring.** This pin can be used as either a temperature sense pin or a current monitoring pin. If this pin is configured as IMON, it can monitor the battery charging current in charge mode, and the discharging current in source mode.
8	VNTC	**Battery temperature-sense bias.** The VNTC pin is used as the voltage bias of the NTC comparator resistor divider for both the feedback and reference.
9, 10	NTC	**Negative temperature coefficient thermistor pin.** The NTC pin is the battery temperature-sense input.
11	$\overline{\text{ACOK}}$	**Input power good indication.** This pin is an open-drain output that indicates when the adapter is present. This pin must be pulled up to VCC via an external 10kΩ resistor.
12	BATT	**Battery pin.** Connect the BATT pin to the battery pack's positive terminal. It is recommended to use two 22μF ceramic capacitors. To reduce IR drop, place the battery as close as possible to the BATT pin.
13	BGATE	**Battery N-channel MOSFET gate driver.** The BGATE pin drives the N-channel MOSFET between the SYS and BATT pins.
14	SRN	**Sense resistor negative terminal.**
15, 16	SRP	**Sense resistor positive terminal.**
17	BST2	**Bootstrap.** Connect a 100nF bootstrap capacitor between the BSTx and SWx pins to form a floating supply across the power switch driver. This drives the power MOSFET's gate above the supply voltage.
23	BST1	
18	SYS	**System pin.** SYS is the power output of the MP2760. Place a 1μF ceramic capacitor from SYS to PGND, and as close as possible to the IC. It is recommended to use four 22μF ceramic capacitors and one 1μF ceramic capacitor.
19	SW2	**Switching node.** SW2 is the middle point of the boost phase's half-bridge.
20	PGND	**Power ground.**
21	SW1	**Switching node.** SW1 is the middle point of the buck phase's half-bridge.
22	IN	**Input pin.** IN is the power stage input of the IC. It is recommended to place four 10μF ceramic capacitors at IN.
24, 25	IAN	**Input current-sense negative terminal.**
26	IAP	**Input current-sense positive terminal.**
27	ACGATE	**Input N-channel MOSFET gate driver.** The ACGATE pin drives the external pass-through N-channel MOSFET. Connect a 1MΩ resistor between ACGATE and the N-channel MOSFET's source port.

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
28	ADP	**Adapter voltage sense.** If the ADP over-voltage protection (OVP) threshold is reached, an external OVP MOSFET (if available) is turned off by the ACGATE driver, and the power stage is disabled. The MP2760 should draw its internal biased voltage from ADP. It is recommended to place one 10μF ceramic capacitor at ADP.
29	FB	**Feedback.** In source mode, FB is the IN output voltage in source mode (V_{IN_SRC}) feedback pin. If V_{IN_SRC} feedback is configured via the register, this pin is not functional. Float FB or connect it to AGND.

ABSOLUTE MAXIMUM RATINGS (1)

ADP, ACGATE to PGND .....-0.3V to +28V
IAP, IAN, IN to PGND (DC).....-0.3V to +26V
IAP, IAN, IN to PGND (20ns).....-0.3V to +28V
IAP to IAN .....-3.6V to +3.6V
SW1, SW2 to PGND (DC) .....-0.3V to +24V
SW1, SW2 to PGND (20ns) .....-2V to +28V
SYS, BATT to PGND .....-0.3V to +24V
SRP, SRN to PGND .....-0.3V to +24V
SRP to SRN .....-3.6V to +3.6V
BGATE to PGND .....-0.3V to +26V
BST1 to SW1 ..... 0 to 5V
BST2 to SW2 ..... 0 to 5V
All other pins to AGND.....-0.3V to +5V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (2)
..... 3.29W
Storage Temperature…. ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 2kV
Charged device model (CDM) 750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4V to 22V
Input current (I_{IN}).....Up to 6A
System current (I_{SYS}).....Up to 6A
Charge current (I_{CC}) .....Up to 6A
Battery voltage (V_{BATT}) .....Up to 18.72V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TQFN-30 (4mmx5mm) ..... 38 ..... 8.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0V, V_{BATT} = 3.7V/cell, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Power Characteristics						
Input voltage range	V_{IN}		4		22	V
ADP under-voltage lockout (UVLO) threshold	V_{ADP_UVLO}	V_{ADP} falling	2.4	2.6	2.8	V
ADP UVLO hysteresis		V_{ADP} rising		1		V
ADP over-voltage lockout (OVLO) threshold	V_{ADP_OVP}	V_{ADP} rising	23.3	23.9	24.4	V
ADP OVLO hysteresis		V_{ADP} falling		500		mV
ADP over-voltage protection (OVP) recovery deglitch time		V_{ADP} falling		100		ms
Input UVLO recovery degltich time	t_{INUVLO_DGL}	V_{IN} rising		30		ms
Input under-voltage protection (UVP)	V_{IN_UVP}	V_{IN} falling, REG11h, bits[9:8] = 00	3.0	3.2	3.4	V
		V_{IN} falling, REG11h, bits[9:8] = 01	6.15	6.4	6.65	V
		V_{IN} falling, REG11h, bits[9:8] = 10	11.65	12	12.35	V
		V_{IN} falling, REG11h, bits[9:8] = 11	16.35	16.8	17.15	V
Input UVP threshold hysteresis		V_{IN} rising, REG11h, bits[9:8] = 01, 10, or 11		328		mV
		V_{IN} rising, REG11h, bits[9:8] = 00		490		mV
Input UVP recovery deglitch time	t_{INUVP_DGL}	V_{IN} rising, REG11h, bit[10] = 0		30		ms
Input OVP threshold	V_{IN_OVP}	V_{IN} rising, REG11h, bits[7:6] = 00	7	7.25	7.5	V
		V_{IN} rising, REG11h, bits[7:6] = 01	10.9	11.25	11.6	V
		V_{IN} rising, REG11h, bits[7:6] = 10	17.15	17.65	18.05	V
		V_{IN} rising, REG11h, bits[7:6] = 11	22	22.45	22.9	V
Input OVP deglitch time	t_{INOVP_DGL}	V_{IN} rising, REG11h, bit[10] = 0		1		µs
		V_{IN} rising, REG11h, bit[10] = 1		15		ms
Input OVP hysteresis		V_{IN} falling		320		mV
Input OVP recovery deglitch time		V_{IN} falling		30		ms
DC/DC Converter						
Input quiescent current	I_{IN_Q}	V_{IN} = 5V, buck-boost mode, ACGATE and BGATE are disabled		550	620	µA
		V_{IN} = 5V/9V, buck-boost mode, BGATE is disabled, ACGATE is enabled		1	1.2	mA
		V_{IN} = 5V/9V, buck-boost mode, BGATE and ACGATE are enabled, charging disabled		7	9.1	mA
VCC LDO output voltage	V_{VCC}	V_{IN} = 5V, I_{VCC} = 15mA		3.6		V
VCC LDO current limit	I_{VCC}	V_{IN} = 5V, V_{VCC} = 3.3V		23		mA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.7V/cell, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
IN to SW1 N-channel MOSFET (Q1) on resistance	R_{ON_Q1}			10		mΩ
SW1 to PGND N-channel MOSFET (Q2) on resistance	R_{ON_Q2}			8		mΩ
SYS to SW2 N-channel MOSFET (Q3) on resistance	R_{ON_Q3}			8		mΩ
SW2 to PGND N-channel MOSFET (Q4) on resistance	R_{ON_Q4}			20		mΩ
Operation frequency	f_{SW}	REG0Eh, bits[6:4] = 000	450	500	550	kHz
		REG0Eh, bits[6:4] = 001	540	600	660	kHz
		REG0Eh, bits[6:4] = 010	630	700	770	kHz
		REG0Eh, bits[6:4] = 100	675	750	825	kHz
		REG0Eh, bits[6:4] = 011	720	800	880	kHz
		REG0Eh, bits[6:4] = 101	810	900	990	kHz
		REG0Eh, bits[6:4] = 110	900	1000	1100	kHz
		REG0Eh, bits[6:4] = 111	1070	1200	1280	kHz
Minimum system voltage setting	V_{SYS_MIN}	1 cell OTP code setting, REG07h, bits[6:0] = 001 0010	3.53	3.6	3.69	V
		2 cells OTP code setting, REG07h, bits[6:0] = 010 0000	6.2	6.4	6.6	V
		2 cells OTP code setting, REG07h, bits[6:0] = 010 0100	7	7.2	7.4	V
		3 cells OTP code setting, REG07h, bits[6:0] = 010 1101	8.73	9	9.27	V
		4 cells OTP code setting, REG07h, bits[6:0] = 011 1100	11.64	12	12.36	V
Battery track regulation voltage	V_{TRACK}	T_A = 25°C, 1 cell OTP code setting, REG10h, bits[4:0] = 10100, REG10h, bits[10:9] = 00	45	100	180	mV
		T_A = 0 to 70°C, 1 cell OTP code setting, REG10h, bits[4:0] = 10100, REG10h, bits[10:9] = 00	40	100	185	mV

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.7V/cell, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Battery track regulation voltage	V_{TRACK}	T_A= 25°C, 2 cells OTP code setting, REG10h, bits[4:0] = 10100, REG10h, bits[10:9] = 01	115	200	370	mV
		T_A= 0 to 70°C, 2 cells OTP code setting, REG10h, bits[4:0] = 10100, REG10h, bits[10:9] = 01	110	200	375	mV
		T_A= 25°C, 3 cells OTP code setting, REG10h, bits[4:0] = 10100, REG10h, bits[10:9] =10		300		mV
		T_A= 25°C, 4 cells OTP code setting, REG10h, bits[4:0] = 10100, REG10h, bits[10:9] = 11		430		mV
SYS OVP threshold	V_{SYS_OV}	V_{SYS} rising, as a percentage of V_{SYS} regulation, REG11h, bits[14:13] = 11		110		%
SYS OVP hysteresis		V_{SYS} falling		5		%
SYS UVP threshold	V_{SYS_UV}	V_{SYS} falling, as a percentage of V_{SYS} regulation, REG11h, bits[12:11] = 00		75		%
SYS UVP hysteresis		V_{SYS} falling, as a percentage of V_{SYS} regulation		5		%
SYS UVP deglitch time	t_{SYSUVP_DGL}	V_{SYS} falling		10		ms
SYS UV recovery deglitch time		V_{SYS} rising		375		ms
Battery Charger						
Battery charge voltage regulation range	V_{BATT_REG}	1-cell OTP code setting	3.4		4.68	V
		2-cell OTP code setting	6.8		9.36	V
		3-cell OTP code setting	10.2		14.04	V
		4-cell OTP code setting	13.6		18.72	V
Battery charge voltage regulation accuracy		T_A = 25°C, V_{BATT_REG} = 4.35V, 1-cell OTP code setting	-0.5		+0.5	%
		T_A = 0°C to 70°C, V_{BATT_REG} = 4.35V, 1-cell OTP code setting	-0.7		+0.7	%
		T_A = 25°C, V_{BATT_REG} = 8.4V, 2-cell OTP code setting	-0.5		+0.5	%
		T_A = 0°C to 70°C, V_{BATT_REG} = 8.4V, 2-cell OTP code setting	-0.7		+0.7	%
		T_A = 25°C, V_{BATT_REG} = 12.6V, 3-cell OTP code setting	-0.5		+0.5	%
		T_A = 0°C to 70°C, V_{BATT_REG} = 12.6V, 3-cell OTP code setting	-0.7		+0.7	%
		T_A = 25°C, V_{BATT_REG} = 16.8V, 4-cell OTP code setting	-0.5		+0.5	%
		T_A = 0°C to 70°C, V_{BATT_REG} = 16.8V, 4-cell OTP code setting	-0.7		+0.7	%

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.7V/cell, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Fast charge current range	I_{CC}		0		6.35	A
Fast charge current (V_{BATT} > V_{SYS_MIN} + V_{TRACK})	I_{CC}	I_{CC} = 6A, V_{BATT} = 7.6V, T_A = 25°C, REG14h, bits[13:6] = 0111 1000	5.850	6.000	6.240	A
		I_{CC} = 3A, REG14h, bits[13:6] = 0011 1100	2.895	3.015	3.190	A
		I_{CC} = 2A, REG14h, bits[13:6] = 0010 1000	1.940	2.030	2.175	A
		I_{CC} = 500mA, T_A= 25°C, REG14h, bits[13:6] = 0000 1010	0.440	0.550	0.660	A
Fast charge current accuracy (V_{BATT} < V_{SYS_MIN})		I_{CC} = 2A, V_{BATT} = 6.2V, V_{SYS_MIN} = 6.4V, V_{TRACK} = 100mV	-10		+10	%
Pre-charge to fast charge threshold	V_{BATT_PRE}	REG0Bh, bit[12] = 1	2.9	3	3.1	V/cell
		REG0Bh, bit[12] = 0	2.45	2.55	2.6	V/cell
Pre-charge to fast charge deglitch time				30		ms
Pre-charge to fast charge hysteresis		1 cell		85		mV
		2 cells		160		mV
		3 cells		240		mV
		4 cells		315		mV
Pre-charge current range	I_{PRE}		0		1.5	A
Pre-charge current accuracy		2 cells, V_{BATT} = 5V, I_{PRE} = 300mA, REG0Fh, bits[7:4] = 0011	-20		+20	%
		2 cells, V_{BATT} = 5V, I_{PRE} = 500mA, REG0Fh, bits[7:4] = 0101	-15		+15	%
Trickle charge to pre-charge threshold	V_{BATT_TC}	V_{BATT} rising		2		V/cell
Trickle charge to pre-charge hysteresis		V_{BATT} falling		200		mV/cell
Trickle charge current range	I_{TC}		0		750	mA
Trickle charge current		2 cells, V_{BATT} = 3V, I_{TC} = 100mA, REG0Fh, bits[11:8] = 0010	65	100	150	mA
Auto-recharge battery voltage threshold		Lower than battery charge voltage, REG10h, bit[11] = 0		120		mV/cell
Battery auto-recharge deglitch time	t_{RECH_DGL}			240		ms
Battery OVP threshold	V_{BATT_OVP}	V_{BATT} rising	170	230	285	mV/cell
Battery OVP hysteresis		V_{BATT} falling		113		mV/cell
Battery OVP deglitch time				30		ms

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.7V/cell, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Total charge and pre-charge timer			1.8	2	2.2	hr
Total charge timer		REG12h, bits[12:11] = 11	18	20	22	hr
Termination current		I_{TERM} = 100mA, 2 cells, V_{BATT} = 8.4V, REG0Fh, bits[3:0] = 0010		100		mA
		I_{TERM} = 200mA, 2 cells, V_{BATT} = 8.4V, REG0Fh, bits[3:0] = 0100		220		mA
		I_{TERM} = 400mA, 2 cells, V_{BATT} = 8.4V, REG0Fh, bits[3:0] = 1000		420		mA
Charge Termination Deglitch Time	t_{TERM_DGL}			1		s
Pin Leakage Current						
SRP, SRN leakage current	$I_{LKG_SRP_SRN}$		-0.5		+0.5	µA
IAP, IAN leakage current	$I_{LKG_IAP_IAN}$		-0.5		+0.5	µA
Input Current and Input Voltage Limit						
Input current limit range	I_{IN_LIM}		0		5.8	A
Input current limit	I_{IN_LIM}	REG08h, bits[6:0] = 000 1010, I_{IN_LIM} = 0.5A, T_A = 25°C	0.368	0.430	0.50	A
		REG08h, bits[6:0] = 001 0010, I_{IN_LIM} = 0.9A	0.768	0.820	0.90	A
		REG08h, bits[6:0] = 001 1110, I_{IN_LIM} = 1.5A	1.322	1.410	1.50	A
		REG08h, bits[6:0] = 011 1100, I_{IN_LIM} = 3.0A, T_A = 25°C	2.762	2.873	2.98	A
		REG08h, bits[6:0] = 110 0100, I_{IN_LIM} = 5.0A, T_A = 25°C	4.688	4.836	4.98	A
Input minimum voltage regulation	V_{IN_MIN}	REG06h, bits[7:0] = 0011 1001, V_{IN_MIN} = 4.56V	4.44	4.58	4.72	V
		REG06h, bits[7:0] =1000 0010, V_{IN_MIN} = 10.4V	10.19	10.40	10.61	V
		REG06h, bits[7:0] =1010 1010, V_{IN_MIN} = 13.6V	13.33	13.60	13.87	V
		REG06h, bits[7:0] =1110 0111, V_{IN_MIN} = 18.48V	18.11	18.48	18.85	V
Thermal Regulation and Protection						
Thermal shutdown rising threshold (5)	T_{J_SHDN}	T_J rising		150		°C
Thermal shutdown hysteresis (5)				20		°C
Thermal regulation threshold	T_{J_REG}	REG0Fh, bits[14:12] = 111		120		°C

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.7V/cell, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Battery Temperature Monitoring						
NTC floating threshold	V_{NTC_FLT}	V_{NTC} rising as a percentage of V_{VNTC}		95		%
NTC floating threshold hysteresis		V_{NTC} falling as a percentage of V_{VNTC}		3		%
NTC cold temp threshold	V_{COLD}	V_{NTC} rising as a percentage of V_{VNTC}, REG0Dh, bits[1:0] = 01	73.5	74.5	75.5	%
NTC cold temp threshold hysteresis		V_{NTC} falling as a percentage of V_{VNTC}		1.2		%
NTC cool temp threshold	V_{COOL}	V_{NTC} rising as a percentage of V_{VNTC}, REG0Dh, bits[3:2] =10	64.2	65.2	66.2	%
NTC cool temp threshold hysteresis		V_{NTC} falling as a percentage of V_{VNTC}		1.2		%
NTC warm temp threshold	V_{WARM}	V_{NTC} falling as a percentage of V_{VNTC}, REG0Dh, bits[5:4] = 01	32.2	33.2	34.2	%
NTC warm temp threshold hysteresis		V_{NTC} rising as a percentage of V_{VNTC}		1.2		%
NTC hot temp threshold	V_{HOT}	V_{NTC} falling as a percentage of V_{NTC}, REG0Dh, bits[7:6] = 10	22.6	23.6	24.6	%
NTC hot temp threshold hysteresis		V_{NTC} rising as a percentage of V_{NTC}		1.2		%
TS Hot	V_{TS}	REG0Dh, bits[12:10] = 011, T_A = 100°C	12.5	13.5	14.5	%
VNTC voltage	V_{VNTC}	T_A = 0 to 70°C	1.26	1.28	1.30	V
Source Mode						
IN output voltage in source mode	V_{IN_SRC}	I_{IN_SRC} = 0A, V_{BATT} = 7.6V REG09h, bits[9:0] = 00 1111 1010	4.85	5	5.15	V
		I_{IN_SRC} = 0A, V_{BATT} = 7.6V REG09h, bits[9:0] = 01 1100 0010	8.82	9	9.18	V
		I_{IN_SRC} = 0A, V_{BATT} = 7.6V, REG09h, bits[9:0] = 10 0101 1000	11.76	12	12.24	V
		I_{IN_SRC} = 0A, V_{BATT} = 7.6V, REG09h, bits[9:0] = 10 1110 1110	14.7	15	15.3	V
		I_{IN_SRC} = 0A, V_{BATT} = 7.6V, REG09h, bits[9:0] = 11 1110 1000	19.7	20	20.3	V
FB reference voltage for external setting	V_{FB}	REG09h, bits[9:0] = 11 1110 1000	1.194	1.206	1.218	V
		REG09h, bits[9:0] = 00 1111 1010	0.306	0.313	0.320	V
Output OVP in source mode	$V_{IN_SRC_OV}$	V_{BATT} = 7.4V, V_{IN_SRC} rising, percentage of output voltage setting in source mode, REG11h, bits[14:13] = 11		110		%
Output OVP hysteresis in source mode		V_{IN_SRC} falling		5		%
Output UVP in source mode	$V_{IN_SRC_UV}$	REG11h, bits[12:11] = 00		75		%

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.7V/cell, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output UVP hysteresis in source mode				5		%
Output UV deglitch time in source mode	$t_{IN_SRC_UV_DGL}$	V_{IN_SRC} falling		10		ms
Output UV recovery deglitch time in source mode		V_{IN_SRC} rising		30		ms
IN output current regulation in source mode	I_{IN_SRC}	REG0Ah, bits[6:0] = 001 1110, V_{BATT} = 7.4V	900			mA
		REG0Ah, bits[6:0] = 010 1100, V_{BATT} = 7.4V	1500			mA
		REG0Ah, bits[6:0] = 100 1100, V_{BATT} = 7.4V	3000			mA
Battery UVLO threshold	V_{BATT_UVLO}	V_{BATT} falling	2.5	2.6	2.7	V/cell
Battery UVLO hysteresis		V_{BATT} rising		280		mV/cell
Battery low-voltage threshold	V_{BATT_LOW}	V_{BATT} falling, REG0Bh, bits[10:9] = 10	3.1	3.2	3.3	V/cell
Battery low-voltage hysteresis		V_{BATT} rising		200		mV/cell
Battery low-voltage deglitch time		V_{BATT} falling		30		ms
Battery standby current	$I_{BATT_STANDBY}$	V_{IN} = 0V, V_{BATT} = 4.35V, source mode disabled, BGATE disabled, ACGATE disabled, T_A = 25°C	24	28.3	33.8	μA
		V_{IN} = 0V, V_{BATT} = 4.35V, source mode disabled, BGATE disabled, ACGATE disabled, T_A = 0°C to 70°C	23	28.3	36.8	μA
		V_{IN} = 0V, V_{BATT} = 8.4V, source mode disabled, BGATE disabled, ACGATE disabled	28	33	39.3	μA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.7V/cell, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Battery quiescent current	I_{BATT_Q}	V_{IN} = 0V, V_{BATT} = 4.35V, source mode disabled, BGATE is enabled, ADC off, clock off, ACGATE disabled		600	690	μA
		V_{IN} = 0V, V_{BATT} = 8.4V, source mode disabled, BGATE is enabled, ADC off, clock off, ACGATE disabled		70	81.8	μA
		V_{IN} = 0V, V_{BATT} = 4.35V, source mode disabled, BGATE is enabled, ADC on, clock on, ACGATE disabled			1.5	mA
		V_{IN} = 0V, V_{BATT} = 8.4V, source mode disabled, BGATE is enabled, ADC off, clock on, ACGATE disabled			0.655	mA
		V_{BATT} = 4.35V, source mode disabled, BGATE is enabled, ADC on, clock on, ACGATE disabled, IN floating			5	mA
		V_{IN} = 0V, V_{BATT} = 8.4V, source mode disabled, BGATE is enabled, ADC on, clock on, ACGATE disabled, IN floating			5	mA
BGATE and ACGATE Driver						
BGATE	V_{BGATE}	1 cell, V_{BATT} = 4.35V, above V_{SYS} when enabled	4			V
		2 cells, V_{BATT} = 8.4V, above V_{SYS} when enabled	6			V
		Above V_{SYS} when disabled	0			V
ACGATE	V_{ACGATE}	Above V_{ADP} when enabled		6		V
		Above V_{ADP} when disabled		0		V
Open-Drain Pin Characteristics (INT, ACOK)						
Logic low voltage threshold	V_L	I_{SINK} = 10mA			0.4	V
Analog-to-Digital Converter (ADC)						
Sample rate				50		kHz
ADC reference				1.28		V
ADC resolution				10		bits

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.7V/cell, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SMBus Interface (SMBus Should Support I²C Specifications. I²C/SMBus Lines are Compatible with 1.8V/3.3V/5V Logic)						
Input high threshold level	V_{IH}	V_{PULL_UP} = 1.8V, SDA and SCL	1.3			V
Input low threshold level	V_{IL}	V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output low threshold level	V_{OL}	I_{SINK} = 1mA			0.4	V
Pin leakage current	I_{LEAK}		-0.2		+0.2	µA
SMBus Timing Characteristics (5)						
SMBus clock frequency	f_{SCL}		10		400	kHz
Bus free time		Between a stop and start condition	1.3			µs
Start condition hold time (after which the first clock is generated)			0.6			µs
Start condition set-up time			0.6			µs
Stop condition set-up time			0.6			µs
Data hold time			0			ns
Data set-up time			100			ns
Clock low timeout			25		35	ms
Clock low period			1.3			µs
Clock high period			0.6		50	µs
Clock/data falling time					300	ns
Clock/data rising time					300	ns

Notes:

5) Guaranteed by design.

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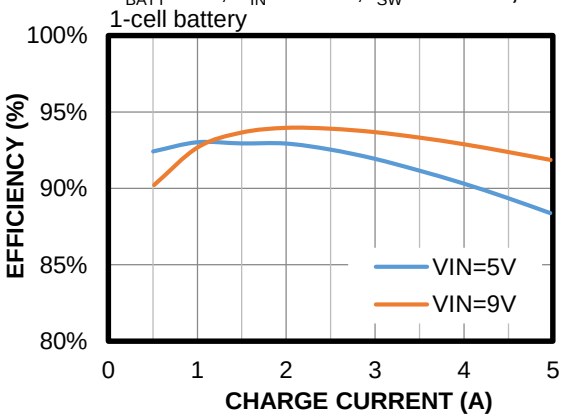
TYPICAL CHARACTERISTICS

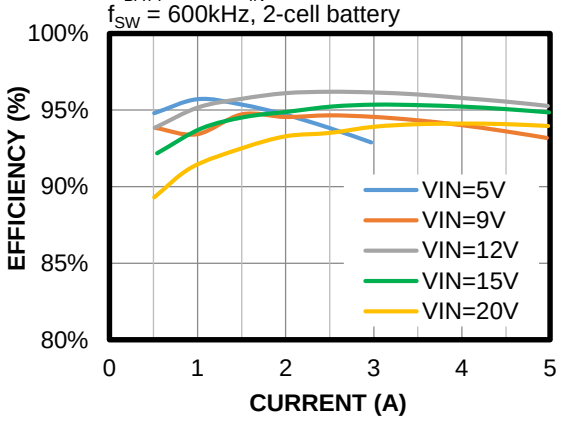
Efficiency vs. Charge Current in Charge Mode

V_{BATT} = 4V, V_{IN} = 5V/9V, f_{SW} = 600kHz, 1-cell battery



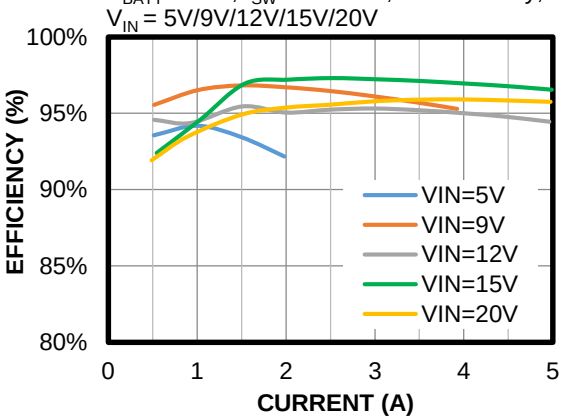
Efficiency vs. Charge Current in Charge Mode

V_{BATT} = 8V, V_{IN} = 5V/9V/12V/15V/20V, f_{SW} = 600kHz, 2-cell battery



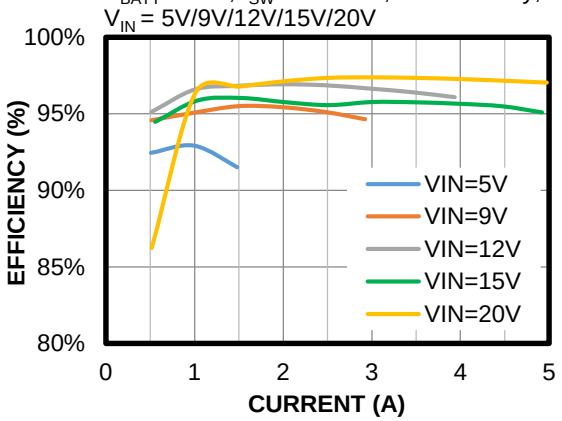
Efficiency vs. Charge Current in Charge Mode

V_{BATT} = 12V, f_{SW} = 600kHz, 3-cell battery, V_{IN} = 5V/9V/12V/15V/20V



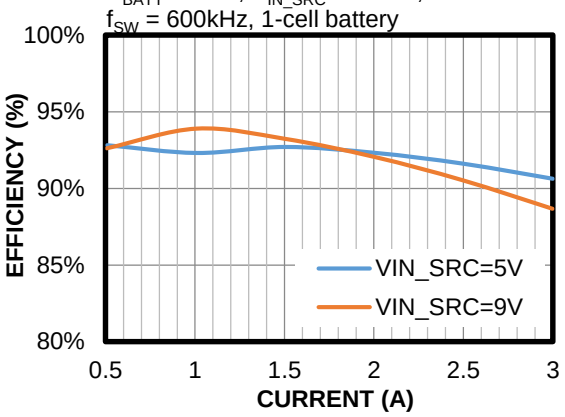
Efficiency vs. Charge Current in Charge Mode

V_{BATT} = 16V, f_{SW} = 600kHz, 4-cell battery, V_{IN} = 5V/9V/12V/15V/20V



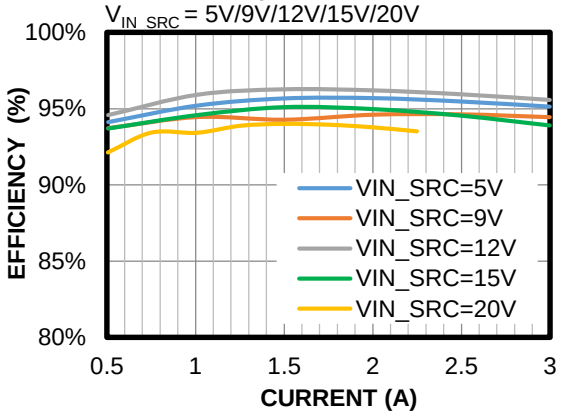
Efficiency vs. Source Current in Source Mode

V_{BATT} = 4.2V, V_{IN_SRC} = 5V/9V, f_{SW} = 600kHz, 1-cell battery



Efficiency vs. Source Current in Source Mode

V_{BATT} = 8.4V, f_{SW} = 600kHz, 2-cell battery, V_{IN_SRC} = 5V/9V/12V/15V/20V



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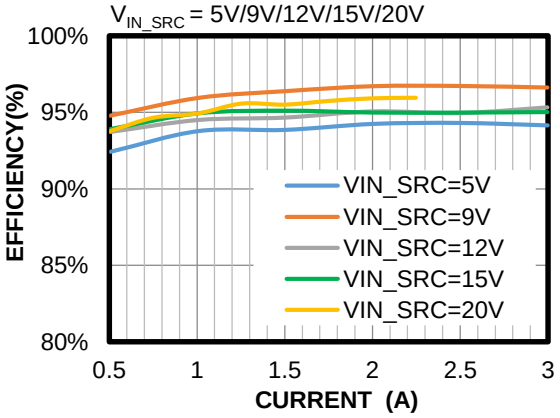
TYPICAL CHARACTERISTICS *(continued)*

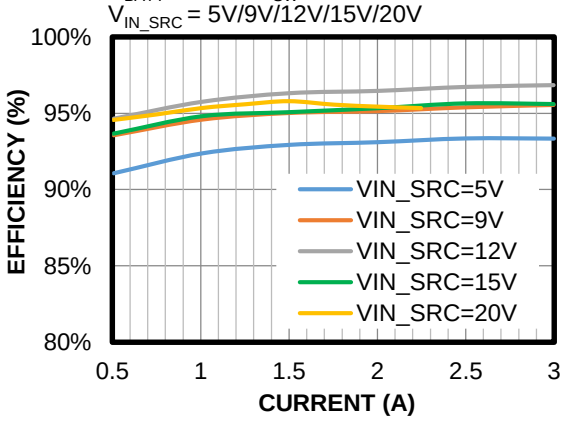
Efficiency vs. Source Current in Source Mode

V_{BATT} = 12.6V, f_{SW} = 600kHz, 3-cell battery, V_{IN_SRC} = 5V/9V/12V/15V/20V



Efficiency vs. Source Current in Source Mode

V_{BATT} = 16.8V, f_{SW} = 600kHz, 4-cell battery, V_{IN_SRC} = 5V/9V/12V/15V/20V



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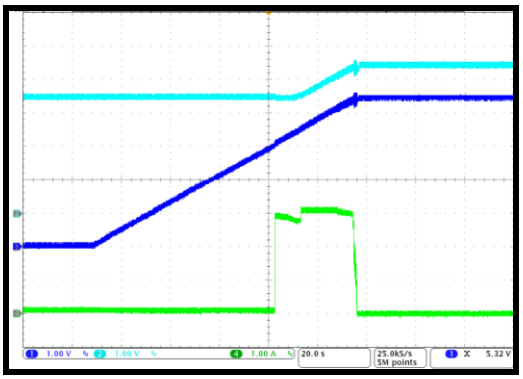
TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN} = 10µF x 5, C_{SYS} = 22µF x 4, C_{BATT} = 22µF x 2, L1 = 1.5µH, f_{SW} = 600kHz, I_{IN_LIM} = 3000mA, I_{CC} = 3100mA, unless otherwise noted.

Charge Profile

5V/3A input, V_{BATT_REG} = 4.35V (1 cell), I_{CC} = 3.1A, battery simulator with 10mV/step

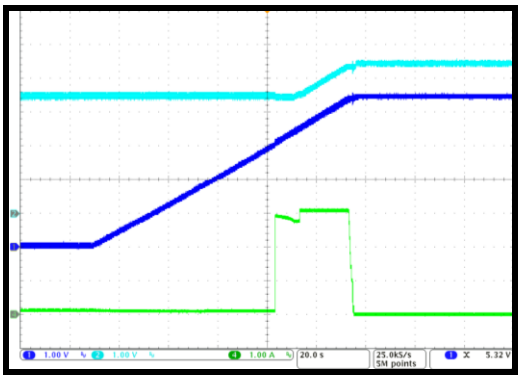
CH2: V_{SYS}
CH1: V_{BATT}
CH4: I_{BATT}



Charge Profile

9V/3A input, V_{BATT_REG} = 4.35V (1 cell), I_{CC} = 3.1A, battery simulator with 10mV/step

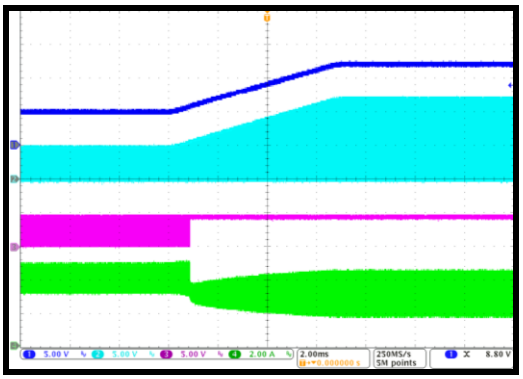
CH2: V_{SYS}
CH1: V_{BATT}
CH4: I_{BATT}



V_{IN} Step from 5V to 12V

V_{BATT} = 4V (1 cell), I_{CC} = 2A, charge enabled

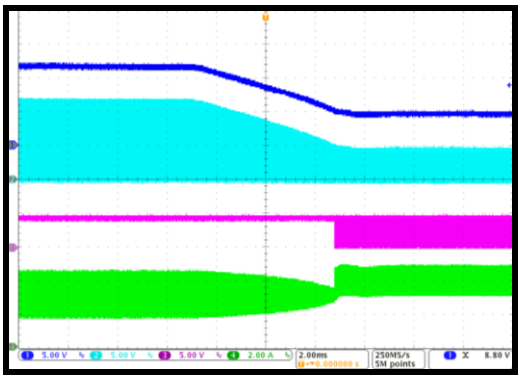
CH1: V_{IN_ADP}
CH2: SW1
CH3: SW2
CH4: I_L



V_{IN} Step from 12V to 5V

V_{BATT} = 4V (1 cell), I_{CC} = 2A, charge enabled

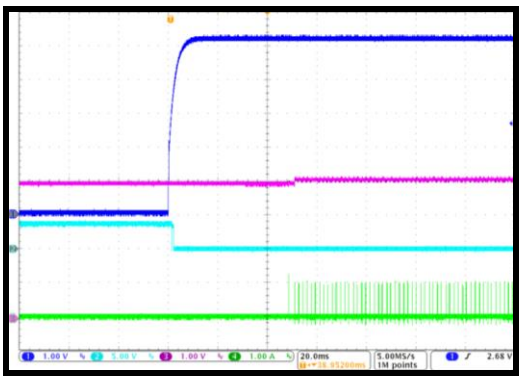
CH1: V_{IN_ADP}
CH2: SW1
CH3: SW2
CH4: I_L



Start-Up through IN

5V input power on, V_{BATT}= 4V (1 cell), charge disabled, I_{SYS} = 0A

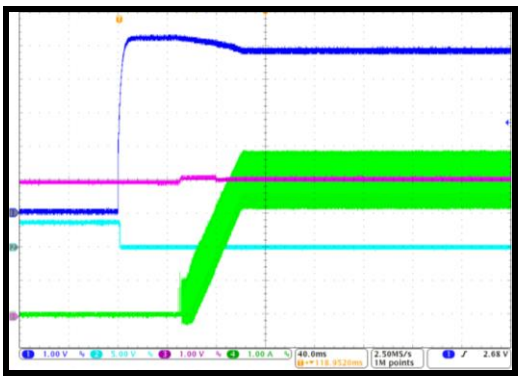
CH1: V_{IN_ADP}
CH2: ACOK
CH3: V_{SYS}
CH4: I_L



Start-Up through IN

5V input power on, V_{BATT} = 4V (1 cell), I_{CC} = 4A, charge enabled, I_{SYS} = 0A

CH1: V_{IN_ADP}
CH2: ACOK
CH3: V_{SYS}
CH4: I_L



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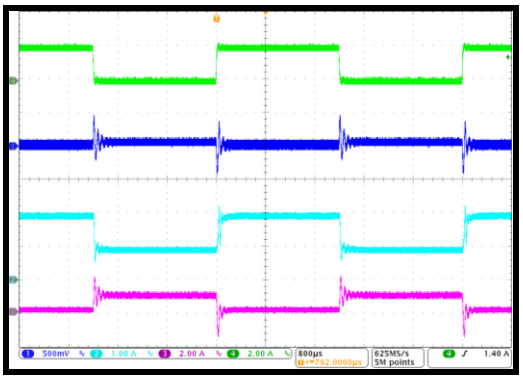
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 10µF x 5, C_{SYS} = 22µF x 4, C_{BATT} = 22µF x 2, L1 = 1.5µH, f_{SW} = 600kHz, I_{IN_LIM} = 3000mA, I_{CC} = 3100mA, unless otherwise noted.

I_{IN_LIM} Transient Response

5V input, I_{IN_LIM} = 2A, V_{BATT} = 4V (1 cell), I_{CC} = 1A, charge enabled, I_{SYS} = 0A to 2A

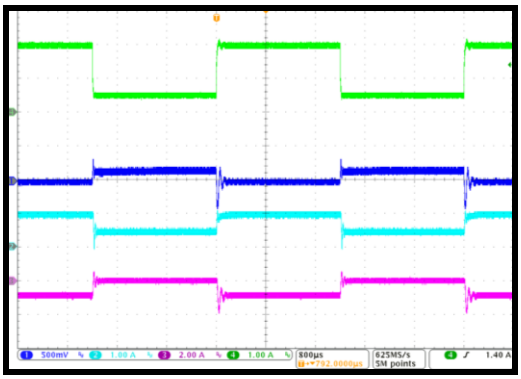
CH4: I_{SYS}
CH1: V_{SYS} (4V offset)
CH2: I_{IN}
CH3: I_{BATT}



I_{IN_LIM} Transient Response

5V input, I_{IN_LIM} = 2A, V_{BATT} = 4V (1 cell), I_{CC} = 1A, charge disabled, I_{SYS} = 0.5A to 1.5A

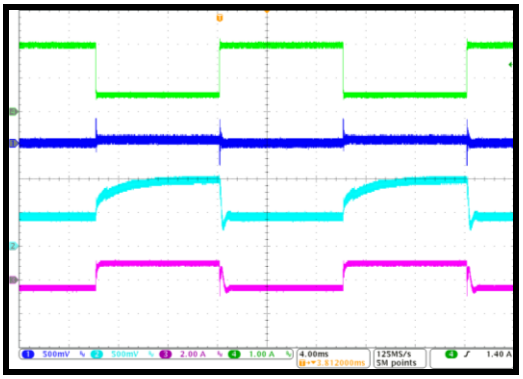
CH4: I_{SYS}
CH1: V_{SYS}
CH2: I_{IN}
CH3: I_{BATT}



V_{IN_MIN} Transient Response

5V/1A input, V_{IN_MIN} = 4.4V, V_{BATT} = 4V (1 cell), I_{CC} = 1A, charge enabled, I_{SYS} = 0.5A to 2A

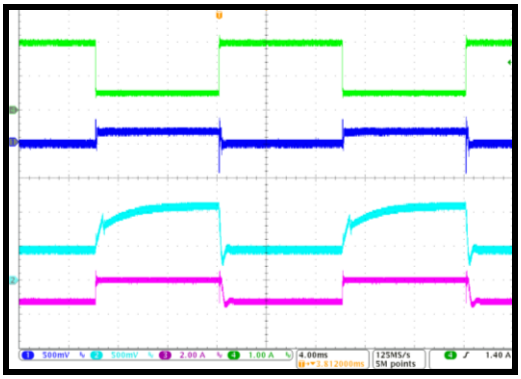
CH4: I_{SYS}
CH1: V_{SYS} (4V offset)
CH2: V_{IN} (4V offset)
CH3: I_{BATT}



V_{IN_MIN} Transient Response

5V/1A input, V_{IN_MIN} = 4.4V, V_{BATT} = 4V (1 cell), I_{CC} = 1A, charge disabled, I_{SYS} = 0.5A to 2A

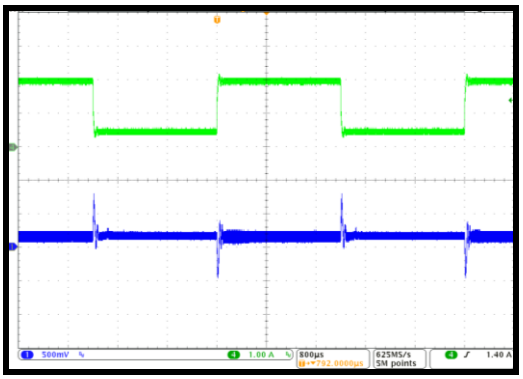
CH4: I_{SYS}
CH1: V_{SYS} (4V offset)
CH2: V_{IN} (4V offset)
CH3: I_{BATT}



System Load Transient

5V input, V_{BATT} = 4V (1 cell), charge disabled, I_{SYS} = 0.5A to 2A

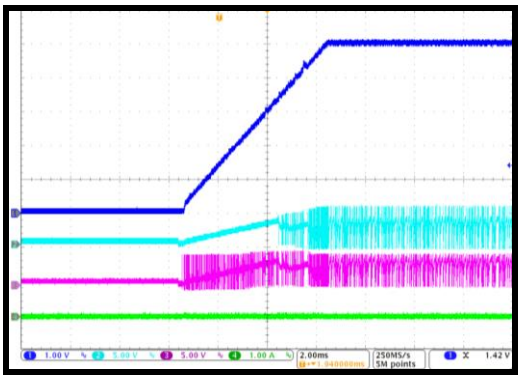
CH 4: I_{SYS}
CH1: V_{SYS} (4V offset)



V_{IN_SRC} Start-Up in Source Mode

V_{BATT} = 4V (1 cell), V_{IN_SRC} = 5V, no load current

CH1: V_{IN_SRC}
CH2: SW1
CH3: SW2
CH4: I_L



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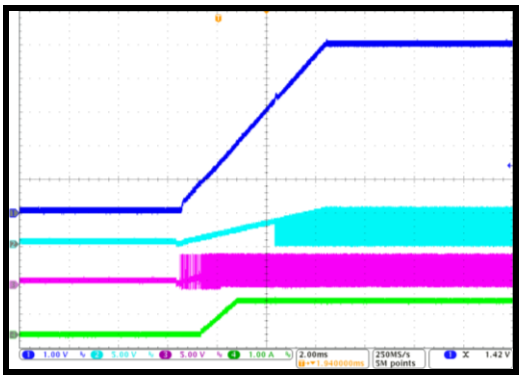
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 10µF x 5, C_{SYS} = 22µF x 4, C_{BATT} = 22µF x 2, L1 = 1.5µH, f_{SW} = 600kHz, I_{IN_LIM} = 3000mA, I_{CC} = 3100mA, unless otherwise noted.

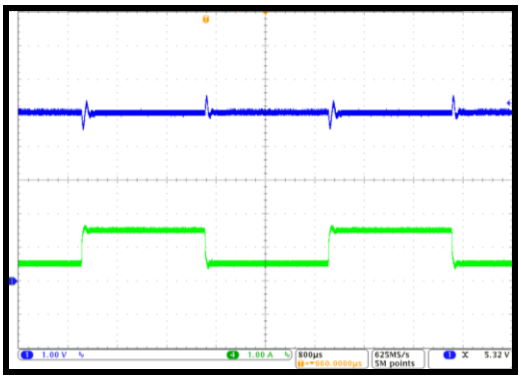
V_{IN_SRC} Start-Up in Source Mode

V_{BATT} = 4V (1 cell), V_{IN_SRC} = 5V, 0.5A load current



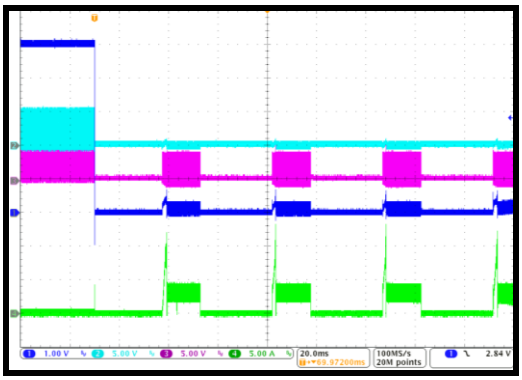
Load Transient in Source Mode

V_{BATT} = 4V (1 cell), V_{IN_SRC} = 5V, load current between 0.5A and 1.5A



V_{IN_SRC} Short in Source Mode

V_{BATT} = 4V (1 cell), V_{IN_SRC} = 5V, no load current



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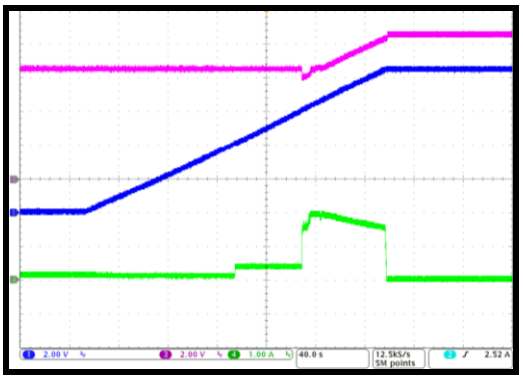
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 10µF x 5, C_{SYS} = 22µF x 4, C_{BATT} = 22µF x 2, L1 = 1.5µH, f_{SW} = 600kHz, I_{IN_LIM} = 3000mA, I_{CC} = 2000mA, 8.4V full, unless otherwise noted.

Charge Profile

5V/3A input, V_{BATT_REG} = 8.4V (2 cell), I_{CC} = 2A, battery simulator with 10mV/step

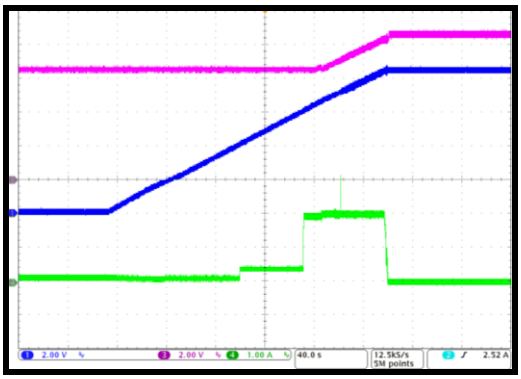
CH3: V_{SYS}
CH1: V_{BATT}
CH4: I_{BATT}



Charge Profile

9V/3A input, V_{BATT_REG} = 8.4V (2 cell), I_{CC} = 2A, battery simulator with 10mV/step

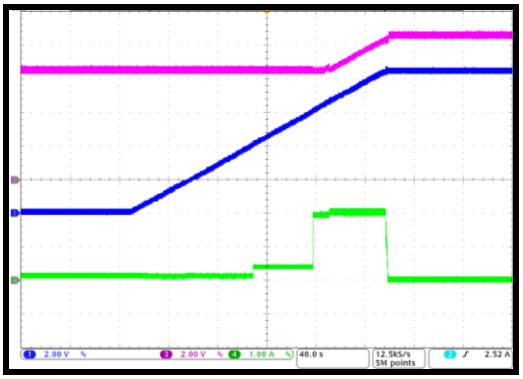
CH3: V_{SYS}
CH1: V_{BATT}
CH4: I_{BATT}



Charge Profile

20/3A input, V_{BATT_REG} = 8.4V (2 cell), I_{CC} = 2A, battery simulator with 10mV/step

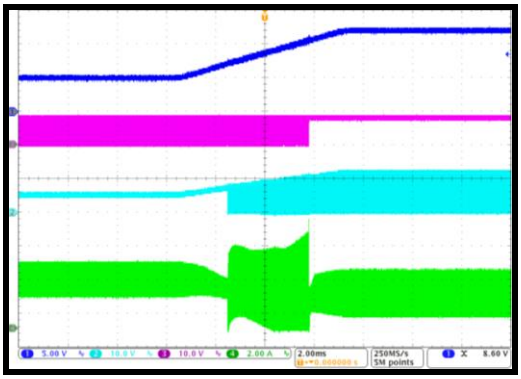
CH3: V_{SYS}
CH1: V_{BATT}
CH4: I_{BATT}



V_{IN} Step from 5V to 12V

V_{BATT} = 7.6V (2 cell), I_{CC} = 2A, charge enabled

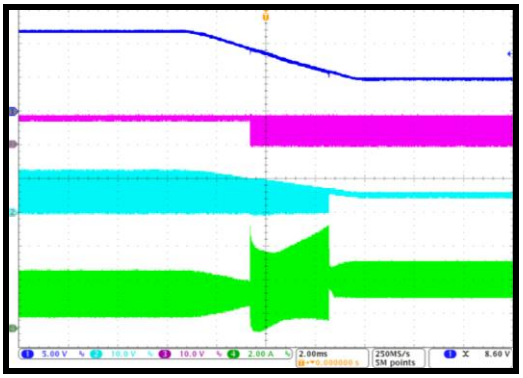
CH1: V_{IN_ADP}
CH3: SW2
CH2: SW1
CH4: I_L



V_{IN} Step from 12V to 5V

V_{BATT} = 7.6V (2 cell), I_{CC} = 2A, charge enabled

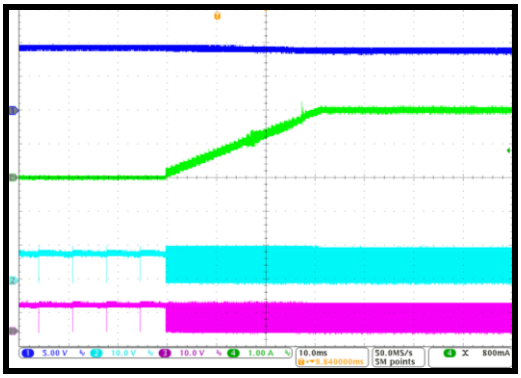
CH1: V_{IN_ADP}
CH3: SW2
CH2: SW1
CH4: I_L



Charge Enabled

9V input, V_{BATT} = 7.4V (2 cell), I_{CC} = 2A

CH1: V_{IN_ADP}
CH4: I_{BATT}
CH2: SW1
CH3: SW2



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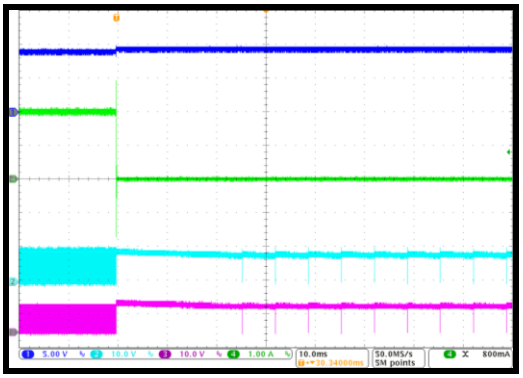
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 10µF x 5, C_{SYS} = 22µF x 4, C_{BATT} = 22µF x 2, L1 = 1.5µH, f_{SW} = 600kHz, I_{IN_LIM} = 3000mA, I_{CC} = 2000mA, 8.4V full, unless otherwise noted.

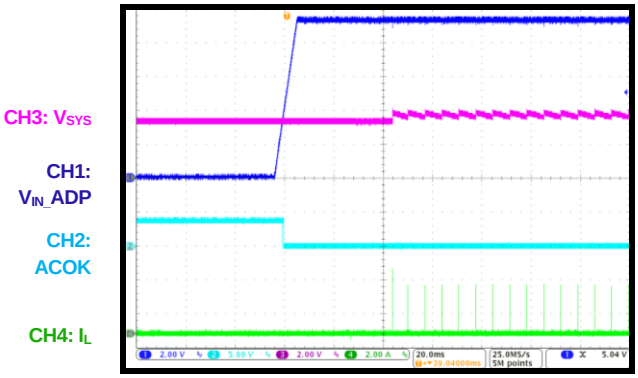
Charge Disabled

9V input, 7.4V (2 cell) and 2A charge



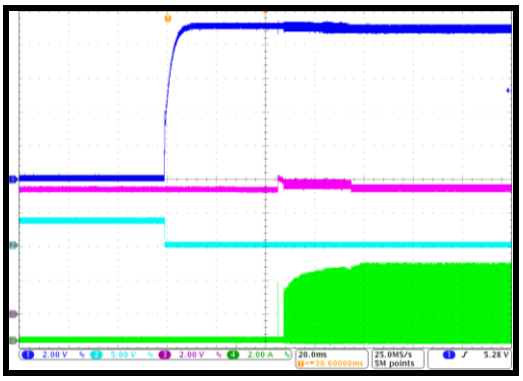
V_{IN} Power On

9V input power on, V_{BATT} = 7.4V (2 cell), I_{CC} = 2A, charge disable, I_{SYS} = 0A



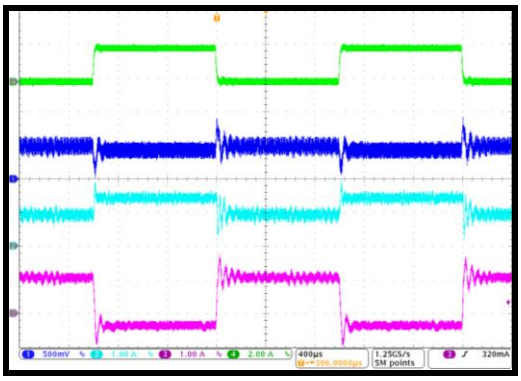
V_{IN} Power On

9V input power on, V_{BATT} = 7.4V (2 cell), I_{CC} = 2A, charge enabled, I_{SYS} = 0A



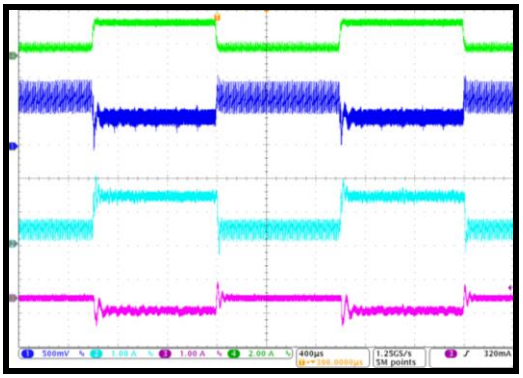
I_{IN_MIN} Transient Response

9V input, I_{IN_MIN} = 1.5A, V_{BATT} = 7.4V (2 cell), I_{CC} = 1A, charge enabled, I_{SYS} = 0A to 2A



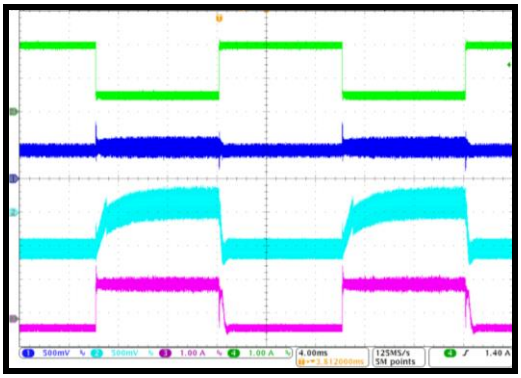
I_{IN_LIM} Transient Response

9V input, I_{IN_MIN} = 1.5A, V_{BATT} = 7.4V (2 cell), charge disabled, I_{SYS} = 0.5A to 2A



V_{IN_MIN} Transient Response

9V/1A input, V_{IN_MIN} = 8.4V, V_{BATT} = 7.4V (2 cell), I_{CC} = 1A, charge enabled, I_{SYS} = 0.5A to 2A



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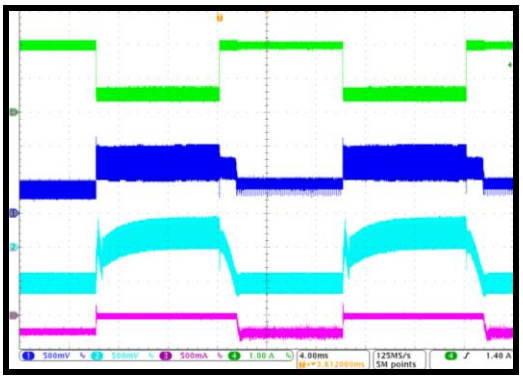
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 10µF x 5, C_{SYS} = 22µF x 4, C_{BATT} = 22µF x 2, L1 = 1.5µH, f_{SW} = 600kHz, I_{IN_LIM} = 3000mA, I_{CC} = 2000mA, 8.4V full, unless otherwise noted.

V_{IN_MIN} Transient Response

9V/1A input, V_{IN_MIN} = 8.4V, V_{BATT} = 7.4V (2 cell), I_{CC} = 1A, charge disabled, I_{SYS} = 0.5A to 2A

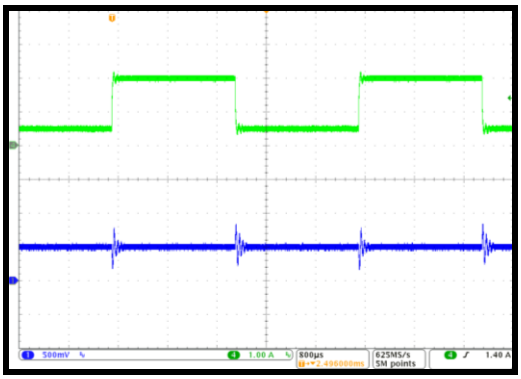
CH4: I_{SYS}
CH1: V_{SYS} (7V offset)
CH2: V_{IN} (9V offset)
CH3: I_{BATT}



System Load Transient

5V input, V_{BATT} = 7.4V (2 cell), charge disabled, I_{SYS} = 0.5A to 2A

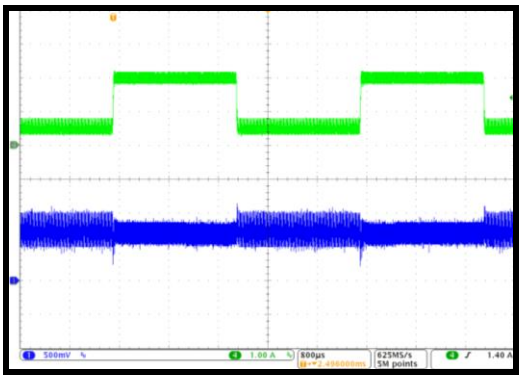
CH4: I_{SYS}
CH1: V_{SYS} (7V offset)



System Load Transient

9V input, V_{BATT} = 7.4V (2 cell), charge disabled, I_{SYS} = 0.5A to 2A

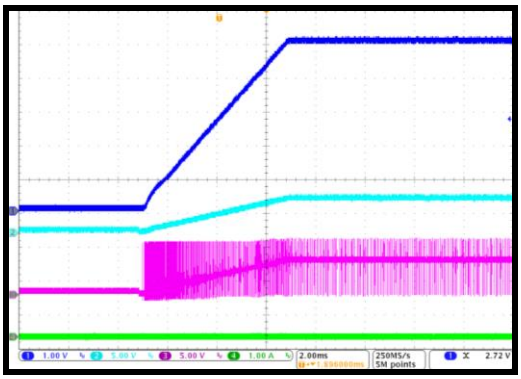
CH4: I_{SYS}
CH1: V_{SYS} (7V offset)



V_{IN_SRC} Start-Up in Source Mode

V_{BATT} = 7.4V (2cell), V_{IN_SRC} = 5V, no load current

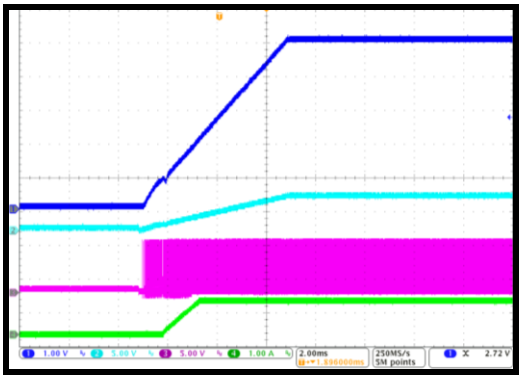
CH1: V_{IN_SRC}
CH2: SW1
CH3: SW2
CH4: I_{SYS}



V_{IN_SRC} Start-Up in Source Mode

V_{BATT} = 7.4V (2 cell), V_{IN_SRC} = 5V, 1A load current

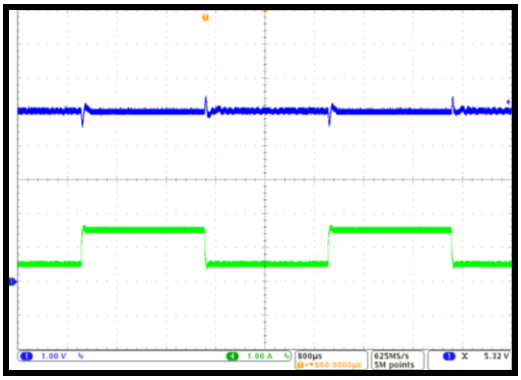
CH1: V_{IN_SRC}
CH2: SW1
CH3: SW2
CH4: I_{SYS}



Load Transient in Source Mode

V_{BATT} = 7.4V (2 cell), V_{IN_SRC} = 5V, load current between 0.5A and 1.5A

CH4: I_{IN_SRC}
CH1: V_{IN_SRC}



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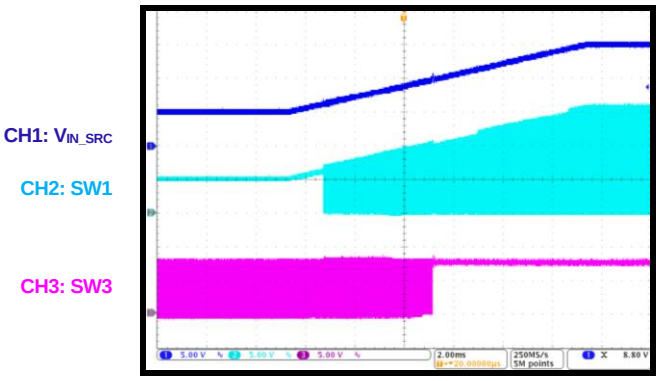
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 10µF x 5, C_{SYS} = 22µF x 4, C_{BATT} = 22µF x 2, L1 = 1.5µH, f_{SW} = 600kHz, I_{IN_LIM} = 3000mA, I_{CC} = 2000mA, 8.4V full, unless otherwise noted.

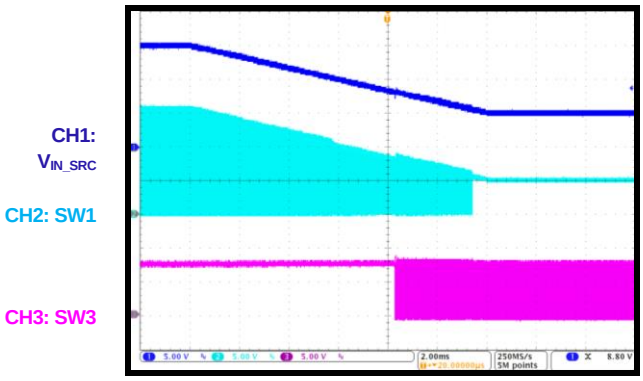
V_{IN_SRC} Step from 5V to 15V

V_{IN_SRC} from 5V to 15V, 1A load current



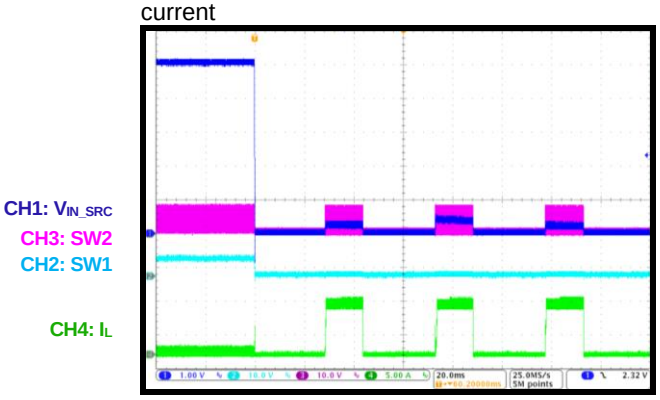
V_{IN_SRC} Step from 15V to 5V

V_{IN_SRC} from 15V to 5V, 1A load current



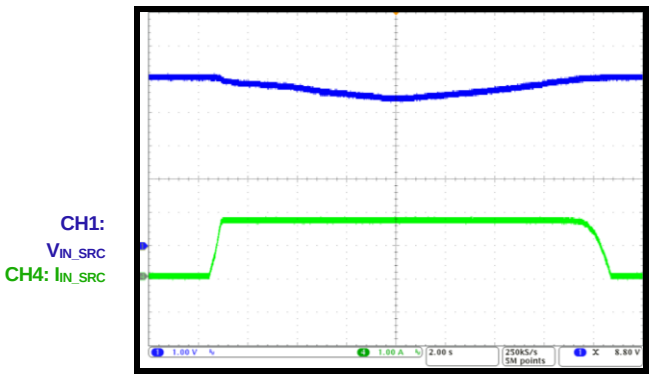
V_{IN_SRC} Short in Source Mode

V_{BATT} = 7.4V (2 cell), V_{IN_SRC} = 5V, no load current



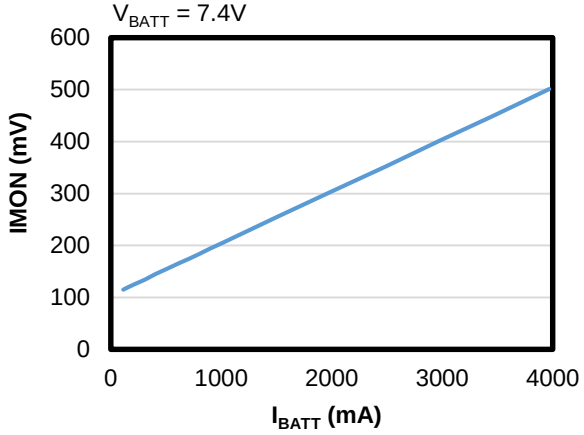
Output Current Limit in Source Mode

V_{BATT} = 7.4V (2 cell), V_{IN_SRC} = 5V, I_{IN_SRC} = 2A



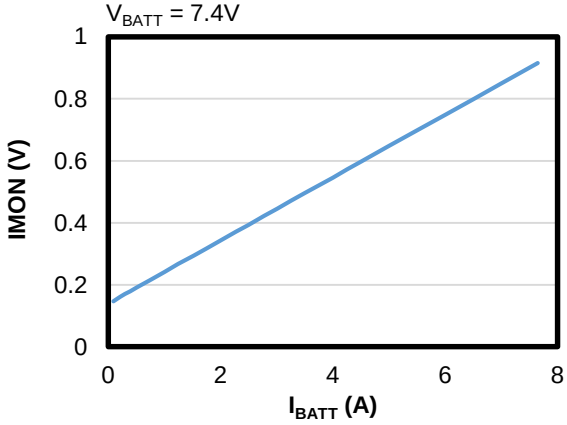
IMON Indicating I_{BATT} in Charge Mode

V_{BATT} = 7.4V



IMON Indicating I_{BATT} in Discharge Mode

V_{BATT} = 7.4V



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FUNCTIONAL BLOCK DIAGRAM

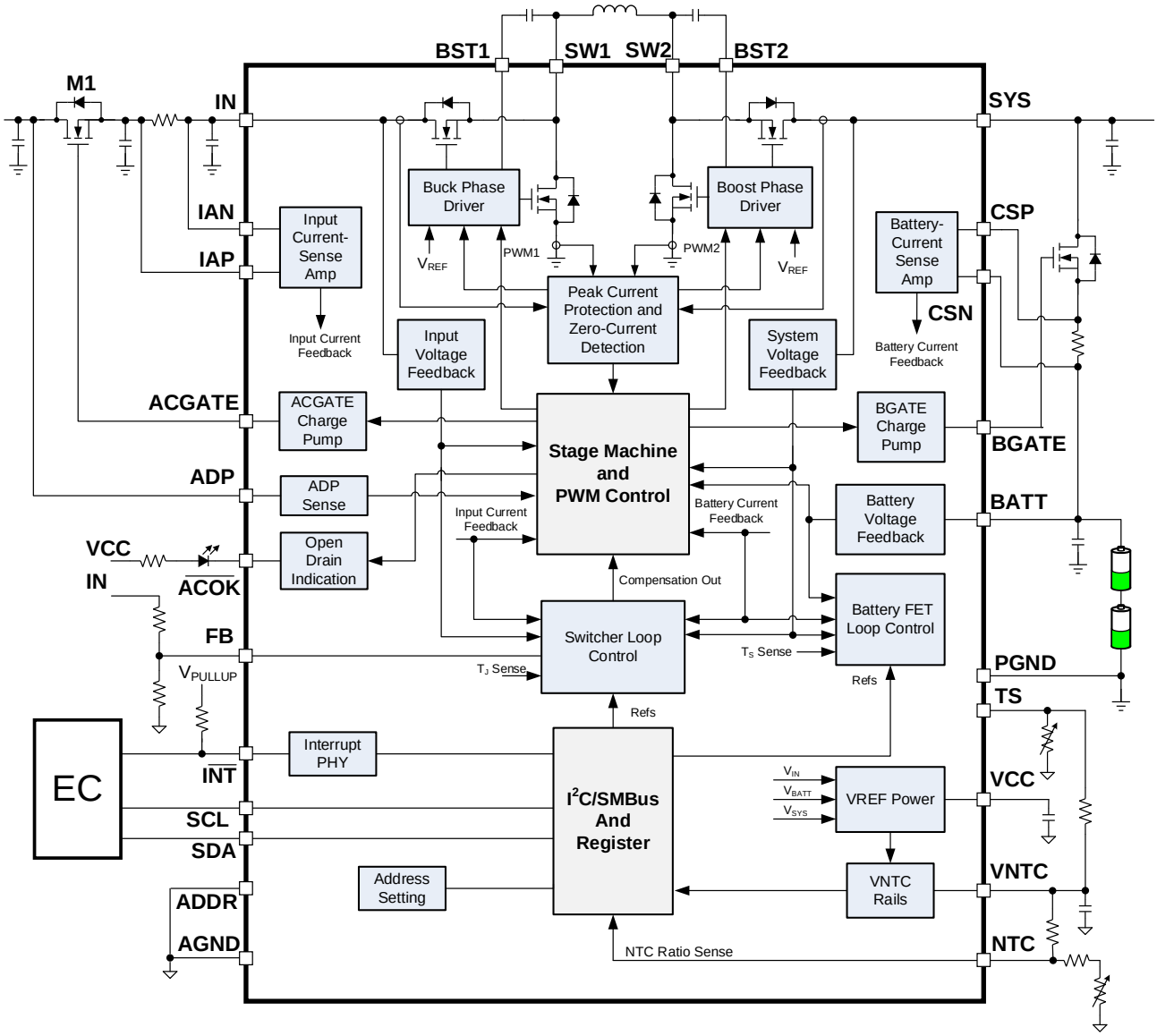

Figure 2: Functional Block Diagram

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OPERATION

Introduction

The MP2760 is a highly integrated buck-boost charger with four switching FETs that charge battery packs with 1 to 4 cells in series. The device also integrates two N-channel MOSFET drivers for input voltage pass-through and NVDC power path control.

The MP2760 can operate in reverse to power the input from the battery. This function is compliant with USB PD source mode.

When the input power is present, the MP2760 operates in charging mode. The buck-boost converter has three operating modes:

- Boost mode when the input voltage is below the battery voltage.
- Buck mode when the input voltage is above the battery voltage.
- Buck-boost mode when the input voltage is almost equal to the battery voltage.

Figure 3 shows the MP2760's power structure.

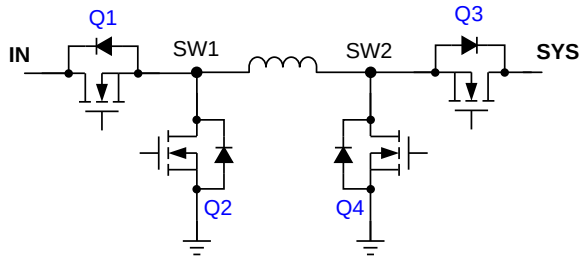

Figure 3: MP2760 Power Stage

Under different operation modes, the MOSFETs (Q1, Q2, Q3, and Q4) operate at different states. Table 1 shows how the MOSFETs operate in charging mode.

Table 1: Q1~Q4 Operation State in Charging Mode

MOSFET	Boost	Buck-Boost	Buck
Q1	On	Switching	Switching
Q2	Off	Switching	Switching
Q3	Switching	Switching	On
Q4	Switching	Switching	Off

Table 2 shows how the MOSFETs operate in source (SRC) mode.

Table 2: Q1~Q4 Operation State in SRC Mode

MOSFET	Boost	Buck-Boost	Buck
Q1	Switching	Switching	On
Q2	Switching	Switching	Off
Q3	On	Switching	Switching
Q4	Off	Switching	Switching

When the input is absent, the MP2760 can operate in reverse to power the input from the battery via I²C/SMBus control. In this scenario, the MP2760 can provide between 4V and 21V of output voltage, with 20mV/step at the input. The device also has a 50mA/step current limit in this mode. Generally, this mode is called source mode in USB PD applications.

When the input is absent and source mode is disabled, the MP2760 operates in standby mode. In standby mode, Q1–Q4 are turned off, and the system is powered by the battery via the external battery FET (BATFET).

VCC LDO Output

The MP2760 integrates an LDO to power the internal circuits, including the I²C block, MOSFET drivers, and biased current. The LDO can also pull up open drains, such as $\overline{\text{ACOK}}$ and $\overline{\text{INT}}$.

VCC is powered by V_{ADP} or V_{BATT}. When $V_{ADP} > V_{ADP_UVLO}$, VCC is powered by V_{ADP} both in charge mode and in source mode. When the input is absent or $V_{ADP} < V_{ADP_UVLO}$, VCC is powered by V_{BATT} while $V_{BATT} > V_{BATT_UVLO}$.

Input Power Status Indication

The MP2760 has both an $\overline{\text{ACOK}}$ pin and status register to indicate whether the input power supply is present. The $\overline{\text{ACOK}}$ pin is an open-drain structure that is pulled to AGND when $V_{IN_UVP} < V_{IN} < V_{IN_OVP}$.

The MP2760 also has status register PG_STAT that reports whether the input voltage is in its normal operation range. This status is only valid in charge mode, or when V_{IN} exceeds V_{IN_UVP} but is below V_{IN_OVP}.

Input Over-Voltage Protection (OVP)

The MP2760 has two tiers for input over-voltage protection (OVP). A dedicated ADP pin

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senses the input voltage. If V_{ADP} > V_{ADP_OVP}, ACGATE is pulled down to turn off M1 immediately. Meanwhile, the buck-boost converter turns off. The MP2760 reports the ADP OVP fault in the fault register. The device has a 100ms deglitch time when recovering from an ADP OVP fault.

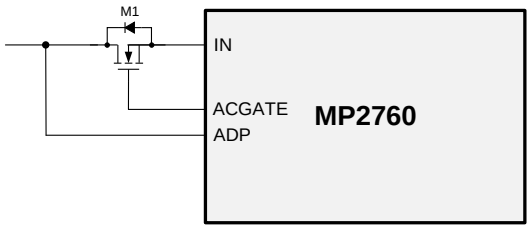

Figure 4: ACGATE Driver

When V_{IN_OVP} < V_{IN} < V_{ADP_OVP}, the M1 turns on and the MP2760's switch is disabled. Then a fault is reported in REG17h, bit[13]. The BATFET turns on if the BATFET block is enabled (REG12h, bit[5] = 1).

Input Current Limit and Input Voltage Limit Regulation

To meet the maximum current limit in the USB specification and avoid overloading the adapter, the MP2760 has both an input current limit and input voltage limit. If either limit is reached, the MP2760 regulates the duty cycle of Q1 and Q4 to limit the input power according to the setting.

NVDC Power Path Management

The MP2760 also provides a BGATE driver to support NVDC power path management. A BGATE driver provides the following features:

- The system instantly starts up after the input power turns on when the battery voltage is low.
- The system voltage stays almost equal to the battery voltage to allow to use of a low voltage point-of-load (POL).
- The battery can supplement the system power when input power is limited.
- When the input is present, the system takes power from the input after charge termination.

Figure 5 shows the NVDC power path structure.

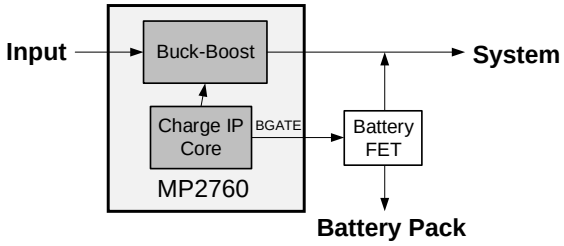

Figure 5: NVDC Power Path Management Structure

The MP2760 can regulate the system voltage at a minimum level even when the battery is depleted. The MP2760 has a V_{SYS_MIN} setting. When charging is disabled (BATFET is off), V_{SYS} is regulated above the maximum values (V_{SYS_MIN}, V_{BATT}) by V_{TRACK}. When V_{BATT} > V_{SYS_MIN}, V_{SYS} always tracks the real battery voltage (see Figure 6).

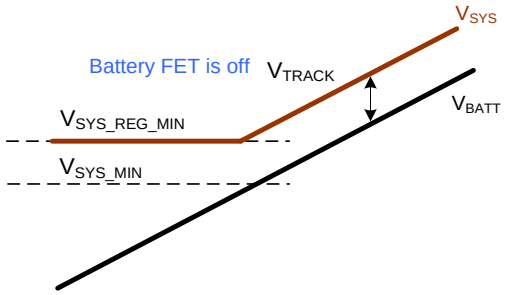

Figure 6: System Voltage Tracking

When charging is enabled, the BATFET fully turns on when V_{BATT} > $V_{SYS_REG_MIN}$ (V_{SYS_MIN} + V_{TRACK}). In this scenario, the charge current loop and battery voltage loop are implemented by the buck-boost converter's PWM control (see Figure 7).

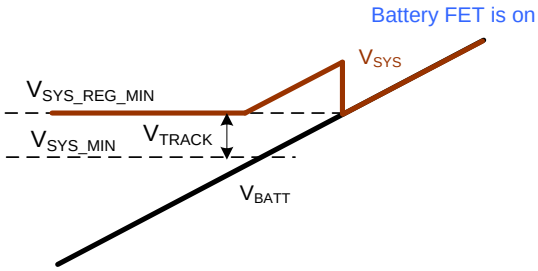

Figure 7: System Voltage Regulation

When V_{BATT} < $V_{SYS_REG_MIN}$ and charging is enabled, the buck-boost converter controls the input current, input voltage, and system voltage loop. Meanwhile, BGATE controls the charge current loop (trickle current charge, pre-charge, and linear CC charge).

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Table 3 summarizes loop control.

Table 3: MP2760 Loop Control Summary

Condition	DC/DC EA	BGATE
$V_{BATT} > V_{SYS_REG_MIN}$	• I_{CC} • V_{BATT_REG} • I_{IN_LIM} • V_{IN_MIN} • T_{J_REG}	• V_{FWD}
$V_{BATT} < V_{SYS_REG_MIN}$	• $V_{SYS_REG_MIN}$ • I_{IN_LIM} • V_{IN_MIN}	• I_{TC} • I_{PRE} • I_{CC} • T_{J_REG} • V_{FWD}
Charge Disabled	• V_{SYS_REG} • I_{IN_LIM} • V_{IN_MIN}	• V_{FWD}

Active Current Foldback

When V_{IN} is sufficiently high and V_{BATT} is below $V_{SYS_REG_MIN}$, the system voltage is regulated at $V_{SYS_REG_MIN}$, and BATFET works linearly to charge the battery with a trickle charge current, pre-charge current, or constant charge current.

If the input current limit or input voltage limit is reached while the system load increases, the system voltage drops. Once V_{SYS} drops by 80mV/cell, BGATE pulls down to reduce the charge current and ensure that the system's power requirements are prioritized.

Battery Supplement Mode

When the input current or input voltage is limited, the charge current is reduced to prevent the input current or input voltage from dropping further. If the input source is still overloaded when the charge current has dropped to zero, the system voltage continues to fall. When the system voltage falls below the battery voltage ($V_{SYS} < V_{BATT}$ - 30mV), the IC enters battery supplement mode. In battery supplement mode, the system load is powered by the battery and DC/DC converter simultaneously.

Virtual Diode Mode Control

Virtual diode mode is designed to optimize the control transition between the battery and the buck-boost converter. In virtual diode mode, BGATE regulates the BATFET's V_{SD} under light discharge current conditions from the battery to the system. The virtual diode mode block is only valid when the input is present.

A comparator compares V_{SYS} to V_{BATT} to determine when the device should enter or exit virtual diode. When $V_{SYS} < V_{BATT}$ - 30mV, virtual diode mode is enabled, and BGATE regulates V_{SD} to 24mV (about V_{FWD}). As the discharge current increases, the battery's gate drive increases while R_{DS} decreases, until the BATFET is fully on. When the system load current drops, V_{SYS} rises above V_{BATT}. The device exits virtual diode mode when $V_{SYS} > V_{BATT}$ + 30mV.

Battery Charge Profile (Supports Linear CC Charge)

In charge mode, the IC has six control loops to regulate the input voltage, input current, charge current, battery charge voltage, system voltage, and the device's junction temperature.

The IC provides four main charging phases: constant current trickle charge, constant current pre-charge, constant current fast charge, and constant voltage charge. Figure 8 on page 29 shows the charging phases.

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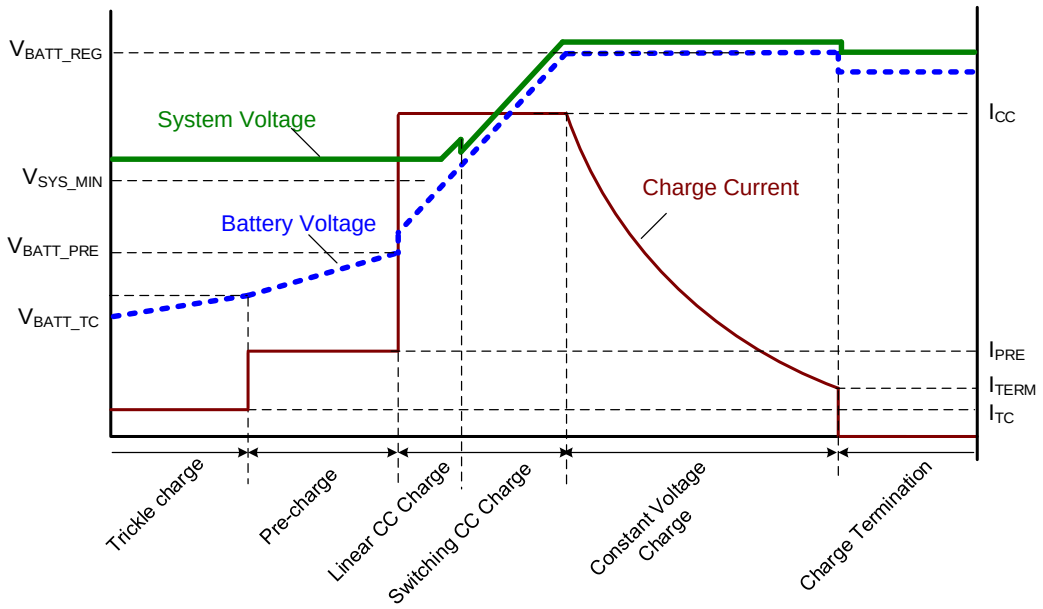

Figure 8: Charge in NVDC Mode

Phase 1 (Constant-Current Trickle Charge)

When the input power qualifies as a good power supply, the IC checks the battery voltage to decide if trickle charging is required. If the battery voltage is below V_{BATT_TC}, a configurable trickle charge current is set to charge the battery.

Phase 2 (Constant-Current Pre-Charge)

When the battery voltage exceeds V_{BATT_TC}, the IC starts to safely pre-charge the deeply depleted battery until the battery voltage reaches the pre-charge to fast charge threshold (V_{BATT_PRE}). If V_{BATT_PRE} is not reached before pre-charge timer (about 2 hours) expires, the charge cycle ends and a corresponding timeout fault signal is asserted. The pre-charge current can be configured via the I²C register REG0Fh, bits[7:4], and V_{BATT_PRE} can be configured via REG0Bh, bit[12]. There are two options for V_{BATT_PRE}: 2.5V/cell for LiFePO4 batteries, and 3.0V/cell for lithium-ion batteries with other chemistries.

Phase 3 (Constant-Current Fast Charge)

When the battery voltage exceeds V_{BATT_PRE} (set via REG0Bh, bit[12]), the IC enters the constant current charge (fast charge) phase. The constant current charge has two different charge modes:

- Linear charge mode when $V_{BATT_PRE} < V_{BATT} < V_{SYS_REG_MIN}$.

  In linear charge mode, V_{SYS} is regulated at $V_{SYS_REG_MIN}$, and the charge current loop is implemented by BGATE.

- Switching charge mode when $V_{BATT} > V_{SYS_REG_MIN}$.

  In switching charge mode, the BATFET is fully on and the charge current loop is implemented by the converter's PWM.

The fast charge current can be configured via REG14h, bits[13:6].

Phase 4 (Constant-Voltage Charge)

When the battery voltage rises to the battery full voltage (V_{BATT_REG}, set via REG15h, bits[14:4]), the charge current begins to taper off.

The charge cycle is considered complete when the charge current reaches the termination threshold (I_{TERM}, set via REG0Fh, bits[3:0]) if the termination function is enabled. If I_{TERM} is not reached before the safety charge timer expires, the charge cycle ends and a corresponding timeout fault signal is asserted. See the Safety Timer section on page 31 for more details.

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Automatic Recharge

When the battery is fully charged and charging is terminated, the battery may be discharged due to system consumption or self-discharge. When the battery voltage is discharged below the configurable recharge threshold, the IC automatically starts a new charging cycle without needing to manually re-start a charging cycle if the input power is valid. The timer resets when the automatic recharge cycle begins.

A new charge cycle can start when all of the following conditions are valid:

- The input power is plugged back in.
- Battery charging is enabled by the I²C/SMBus.
- No thermistor fault has occurred.
- No safety timer fault has occurred.
- No battery over-voltage condition has occurred.
- The BATFET is not forced to turn off.

This means that re-plugging the input power or toggling the battery charging control bit can restart a charge cycle without any fault occurring. The new charge cycle can start with any phase, depending on V_{BATT}.

Battery Over-Voltage Protection (OVP)

The IC provides battery over-voltage protection (OVP). If the battery voltage exceeds the battery over-voltage threshold (230mV above the battery regulation voltage per cell), charging is disabled. Battery OVP has a 30ms deglitch time.

Under this condition, the BATFET turns off and V_{SYS} is regulated at V_{TRACK} + V_{BATT_REG}.

Junction Thermal Regulation

The thermal regulation loop always monitors the internal junction temperature of the IC. If the internal junction temperature exceeds the temperature limit, the charge current is reduced to keep the junction temperature at the regulated threshold. The multiple thermal regulation thresholds (from 80°C to 120°C) help the system design meet the thermal requirements for different applications. The junction temperature regulation threshold can be set via REG0Fh, bits[14:12].

Buck, Buck-Boost, and Boost Mode Transitions

The MP2760 always monitors the input voltage and system voltage. The device automatically switches between different modes according to V_{IN} and V_{SYS} (see Figure 9).

When V_{IN} > 90% x V_{SYS}, the MP2760 transitions from boost mode to buck-boost mode.

When V_{IN} <75% x V_{SYS}, the MP2760 transitions from buck-boost mode to boost mode.

When V_{IN} < 120% x V_{SYS}, the MP2760 transitions from buck mode to buck-boost mode.

When V_{IN} > 135% x V_{SYS}, the MP2760 transitions from buck-boost mode to buck mode.

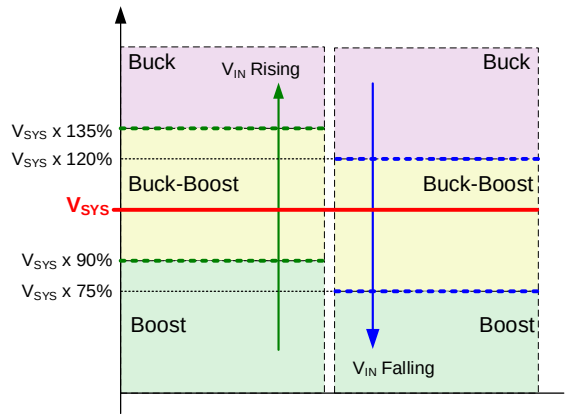

Figure 9: Mode Transition Threshold

Pulse-Skip Mode (PSM)

The MP2760 has PSM control to improve efficiency under light loads. In PSM, a great pulse width is skipped for lighter loads.

Cycle-by-Cycle MOSFET Current Limit

The MP2760 senses the high-side MOSFET (HS-FET) and the low-side (LS-FET) currents during loop control, and provides a valley current limit in buck mode and a peak current limit in boost mode in each switching cycle. In buck mode, the next period does not start before the inductor current (I_L) drops to the valley current limit. I_L rises with a minimum on time, so the device may fold back the frequency when a valley current limit is triggered.

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System Over-Voltage Protection (OVP)

The MP2760 has both over-voltage (OV) and under-voltage protection (UVP) for system voltage regulation.

When $V_{SYS} > V_{SYS_OV}$ (configurable via REG11h, bits[14:13]), the PWM is disabled, and a system OV fault is reported in the status and fault register. The device recovers when V_{SYS} is lower than V_{SYS_OV} by a hysteresis.

System Short-Circuit Protection (SCP)

When the system voltage is below the SYS under-voltage threshold for 10ms, the switcher stops and automatically recovers to the starting point after 375ms. In addition to the 375ms off time, the MP2760 always has a 30ms delay between when the switcher is enabled and the PWM begins operating.

ADC Conversion and Multiplexer

The MP2760 integrates a 10-bit SAR analog-to-digital converter (ADC) with 50kSPS. A 10-channel multiplexer measures certain parameters (see Table 4).

Table 4: ADC Channels

Sink Mode	Source Mode
• Input voltage • Input current • System voltage • Battery voltage • Charge current • Battery temperature (NTC pin voltage ratio) • TS pin voltage ratio • Chip junction temperature	• Output voltage at the IN pin • Output current at the IN pin • System voltage • Battery voltage • Battery discharge current • Battery temperature. • TS pin voltage ratio • Chip junction temperature

There are two conversion modes for the ADC. The first is continuous mode, while the second is one-shot mode. In continuous mode, the ADC keeps running and each parameter is converted to a digital value every 370µs. In one-shot mode, the ADC only converts values once after it is enabled, then the ADC turns off automatically to save power. To use one-shot mode, source mode must be disabled, and only the battery can be connected.

Safety Timer

The IC provides both a linear charger timer and switching constant current constant voltage (CC/CV) timer to prevent extended charging cycles due to abnormal battery conditions. The total safety timer for linear charge (including trickle charge, pre-charge, and linear CC charge) is 2 hours when the battery voltage is below $V_{SYS_REG_MIN}$.

The switching CC/CV charge safety timer starts when the battery enters the switching CC charging phase. The user can configure this timer via REG12h, bits[12:11].

Both safety timers can be disabled via REG12h, bit[13]. The safety timer does not operate in source mode.

The safety timer is reset at the beginning of a new charging cycle. The following actions can also restart the safety timer:

- Automatic recharge (reset when charging ends, restarts when the recharge cycle begins)
- Charge enable toggling (reset when charging is disabled, restarts when charging is enabled)
- Input power toggling (reset if input UVP or OVP occurs)
- USB suspend mode toggling (reset when the converter is disabled, restarts when the converter is enabled)
- Safety timer toggling (reset when the timer is disabled, restarts when the timer is enabled again)
- Thermal shutdown recovery (reset during thermal shutdown, restarts during thermal shutdown recovery)

The IC automatically suspends the timer if either of the following situations occurs:

- Battery supplement mode is initiated
- An NTC hot or cold fault occurs

The IC automatically extends remaining timer duration by two times the original duration if any of the below situations occur:

- The input current limit is reached but the device does not enter battery supplement mode

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- The input voltage limit is reached but the device does not enter battery supplement mode
- There is a thermal loop but the device does not enter battery supplement mode

Once the IC resolves the above events, the timer returns to its standard duration. This function can be disabled via REG12h, bit[10].

Watchdog Timer

The MP2760 has a watchdog timer that monitors the I²C interface. If the watchdog timer is enabled, the host must periodically reset the waterdog timer bit before the watchdog timer expires. If the watchdog timer expires, certain registers are reset to their default values. See the Register Map starting on page 40 to determine which registers are reset after the watchdog timer expires.

The following actions reset the watchdog timer and force the IC to recover from watchdog timer faults:

- Write to the watchdog timer reset bit
- Write to the charge current register (REG14h)
- Write to the charge voltage register. (REG15h)

The watchdog timer can be disabled via REG12h, bits[8:7].

Battery Temperature Monitoring via the NTC Thermistor

Thermally sensitive resistors are generally called thermistors. Negative temperature coefficient (NTC) thermistors are also called thermistors. Depending on the manufacturing method and the structure, there are many types of thermistors for various purposes. Unless otherwise specified, the thermistor resistance values are classified at a standard temperature of about 25°C. The resistance of a thermistor is a function of its absolute temperature.

For more details, refer to the datasheet of the thermistor to determine how resistance and absolute temperature are related. An example can be calculated with Equation (1):

$$R_1 = R_2 \times e^{\beta \times (\frac{1}{T_1} - \frac{1}{T_2})} \quad (1)$$

Where R1 is the resistance at the absolute temperature (T1), R2 is the resistance at the absolute temperature (T2), and β is a constant that depends on the material of the thermistor.

The MP2760 continuously monitors the battery's temperature by measuring the voltage at the NTC pin. This voltage is determined by the resistor divider, which a ratio that is created by the NTC thermistor's different resistances under the battery's different ambient temperatures (see Figure 10).

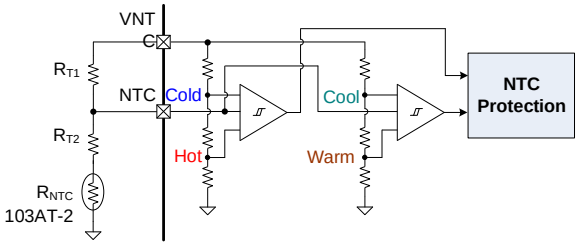

Figure 10: NTC Protection Circuit

The MP2760 internally sets a pre-determined upper and lower bound for this range. If the voltage at the NTC pin goes out of this range, the temperature is outside a safe operating limit. Then charging ends until the operating temperature returns to the safe range.

To satisfy JEITA requirements, the MP2760 has four temperature thresholds: the cold battery threshold (0°C by default), the cool battery threshold (10°C by default), the warm battery threshold (45°C by default), and the hot battery threshold (60°C by default).

For a given NTC thermistor, these temperatures correspond to the V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT} thresholds. which can be configured via REG0Dh, bits[7:0]. When $V_{NTC} < V_{HOT}$ or $V_{NTC} > V_{COLD}$, charging is suspended and the timers are suspended. When $V_{HOT} < V_{NTC} < V_{WARM}$ or when $V_{COOL} < V_{NTC} < V_{COLD}$, the charging behavior can be configured via REG0Ch, bits[14:4]. Figure 11 on page 33 shows the JEITA control profile.

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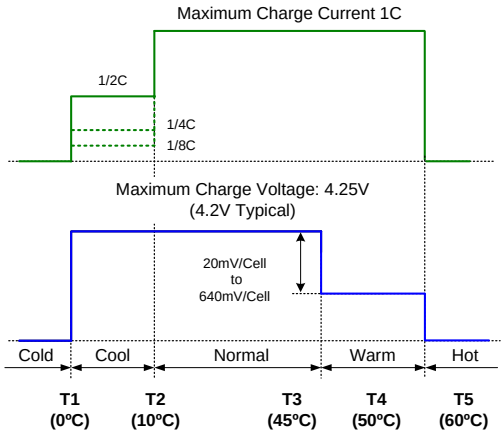

Figure 11: JEITA Control Profile

The MP2760 also monitors the battery temperature in source mode. If the NTC function is enabled, an interrupt (INT) is asserted if the battery temperature is below V_{HOT} or above V_{COLD}.

NTC Floating Detection

If the NTC voltage exceeds 95% of V_{VNTC}, the NTC pin is detected as floating, and an INT asserts to the corresponding status register. When the NTC is floating, BGATE turns off the external BATFET, and the system voltage is regulated to V_{BATT_REG} + V_{TRACK}.

Battery Missing Detection

The MP2760 counts how often charging terminates every 10s. If charging terminates more than three times in 10s, the MP2760 reports that the battery is missing in the status register and initiates an INT signal.

TS/IMON Pin Function

The MP2760 has a TS/IMON pin that monitors either the temperature or current. When REG10h, bit[12] = 0, this pin is configured for temperature monitoring (TS). When REG10h, bit[12] = 1, this pin is used for current monitoring (IMON).

Temperature-Sense (TS) Function

When the temperature-sense (TS) function is enabled, the TS pin can sense either the external BATFET temperature or the input USB connector temperature via REG0Dh, bit[14].

When the TS pin is configured to sense the input connector temperature, and the V_{TS_HOT} threshold (configured via REG0Dh, bits[12:10]) is reached, an INT signal asserts to indicate that a TS fault has occurred. In charging mode, the input current limit drops to 500mA with 50mA/step every 62.5ms. When the IC recovers from a TS fault, the input current limit rises to the set value with 50mA/step every 62.5ms.

When TS is configured to sense the BATFET temperature, and V_{BATT} < $V_{SYS_REG_MIN}$, the IC reduces charging current if BATFET temperature reaches the V_{TS_HOT} threshold. The INT signal asserts to indicate the thermal regulation, though the INT signal can be masked via REG18h.

IMON Function

When the IMON function is enabled, the IMON pin indicates the real-time battery current with a gain of 0.1V/A in charge mode and 0.1V/A in source mode.

Thermal Shutdown

The IC continuously monitors the internal junction temperature to maximize power delivery and avoid overheating the chip. When the junction temperature reaches 150°C, the PWM converter shuts down. The converter does not resume normal operation until the junction temperature drops below 120°C.

Host Mode and Default Mode

The IC is a host-controlled device. After power-on reset (POR), the IC starts in the watchdog timer expiration state or in its default mode. In this scenario, all the registers are under their default settings.

Any write to the IC transits it to host mode, then all the device parameters can be configured by the host. To keep the device in host mode, the host has to reset the watchdog timer regularly by writing 1 to REG12h, bit[9] before the watchdog timer expires. Once the watchdog timer expires, the IC goes back to a default mode.

Impedance Compensation to Accelerate Charging

During the entire charging cycle, the constant voltage charging stage occupies larger ratios. To accelerate the charging cycle ensure that the device stays in the constant current charge stage for as long as possible.

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The IC compensates for the battery's intrinsic resistance by adjusting the battery regulation voltage according to the charge current and internal resistance. In addition, a maximum allowed regulated voltage (V_{CLAMP}) is also set for safe operation. $V_{BATT_REG_ACT}$ can be estimated with Equation (2):

$$V_{BATT_REG_ACT} = V_{BATT_REG} + Min\ (V_{CLAMP}, I_{CHG_ACT} \times R_{BATT}) \quad (2)$$

Where $V_{BATT_REG_ACT}$ is the real battery regulation voltage, V_{BATT_REG} is the battery regulation voltage set via REG15h, bits[14:4], I_{CHG_ACT} is the real-time charge current during the operation, and Min uses the lower value between V_{CLAMP} and (I_{CHG_ACT} x R_{BATT}).

Source Mode Operation

The MP2760 can work in source mode to supply power to the IN pin from the battery. To ensure that the battery is not drained, the IC does not enter this mode if the battery is below the configurable low battery threshold. Source mode can be enabled when REG12h, bit[3] = 1. When both charging and source mode are enabled, source mode takes the higher priority.

In source mode, the IC employs a fixed-frequency (500kHz to 1.2MHz, which can be configured) switching regulator. The device switches from PWM operation to PSM operation under light loads. This operation is similar to system voltage regulation in charge mode.

The IN output voltage in source mode (V_{IN_SRC}) is compliant with USB PD specifications, including 5V, 9V, 15V, and 20V. V_{IN_SRC} can be set by either the internal DAC or the external FB pin. The output current can be configured via the I²C SMBus (up to 5A with 50mA/step).

Source mode is enabled if the following conditions are met:

- $V_{BATT} > V_{BATT_LOW}$
- REG12h, bit[3] = 1

To meet the PD timing specification, V_{IN_SRC} should settle within 275ms in source mode.

In source mode, the DC/DC converter can work in buck mode, boost mode, or buck-boost mode, according to the battery voltage and V_{IN_SRC}.

Output Over-Voltage Protection (OVP) in Source Mode

The MP2760 features output over-voltage protection (OVP) in source mode. The IC continuously monitors the voltage at IN pin in source mode. If $V_{IN} > V_{IN_SRC_OV}$, the PWM is disabled, and an output OVP fault is asserted in the status and fault registers. The PWM recovers when V_{IN} drops below $V_{IN_SRC_OV}$ by a hysteresis.

Output Short-Circuit Protection (SCP) in Source Mode

The IC also features output short-circuit protection (SCP). When the load current reaches the IN output current limit in source mode (I_{IN_SRC}), V_{IAP} starts falling. When V_{IAP} falls below $V_{IN_SRC_UVLO}$ for more than 10ms, the output UVP fault asserts, and source mode is disabled. V_{IAP} restarts after 30ms.

Battery Standby Mode

If only the battery is connected and the input source is absent (and source mode is disabled), the VCC LDO stays on. The IC's maximum quiescent current (I_Q) is 33μA. The low standby current extends the battery's running time.

Battery Under-Voltage Protection (UVP)

The MP2760 has two-level battery under-voltage protection (UVP). In source mode, when $V_{BATT} < V_{BATT_LOW}$ for 30ms, the MP2760 generates an INT signal and reports that the battery voltage is low. Then the MP2760 turns off the buck-boost converter and latches the switcher off. Meanwhile, the external BATFET turns on to power the system from the battery. Only V_{IN} power on again or re-toggling the SRC_EN bit can reset the latch condition.

The MP2760 also has a battery UVLO threshold. When V_{BATT} < 2.45V/cell, the BATFET turns off. When V_{BATT} > (2.45V + 200mV) / cell, there is a 100ms deglitch time before the BATFET turns on.

SMBus and I²C Compatibility

The MP2760 has an SCL/SDA interface that is compatible with the SMBus and I²C. The MP2760's registers are 16 bits, so the device is compatible with both SMBus and the 16-bit I²C.

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The system management bus (SMBus) is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle.

Connecting to the line, a master device generates the SCL signal and device address, then arranges the communication sequence. This is based on the principles of operation of I²C. The MP2760 interface is an SMBus slave device that supports both standard mode (100kHz) and fast mode (400kHz). The SMBus address is 0b0001 001x, where x is 0 (write) or 1 (read). The MP2760 receives control inputs from the master device, such as a microcontroller (MCU) or a digital signal processor.

Start and Stop Commands

All transactions begin with a start (S) command and are terminated by a stop (P) command. Start and stop commands are always generated by the master. A start command is defined as a high-to-low transition on the SDA line while the SCL is high. A stop command is defined as a low-to-high transition on the SDA while the SCL is high (see Figure 12).

Start and stop commands are always generated by the master. The bus is considered busy after the start command; it is considered free after the stop command.

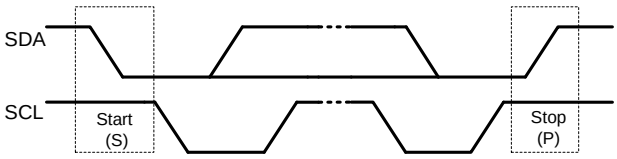


Figure 12: Start and Stop Commands

Data Validity

For data validity, the data on the SDA must be stable during the high period of the clock. The high or low state of the SDA can only change when the clock signal on the SCL is low (see Figure 13). One clock pulse is generated for each data bit transferred.

When the bus is free, both lines are high.

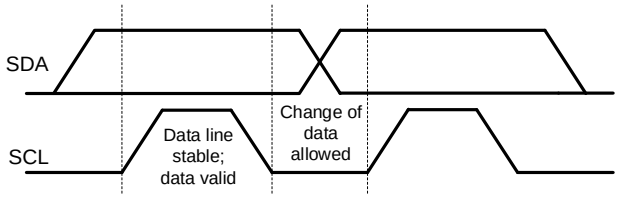


Figure 13: Data Validity

Interrupt to Host (INT)

The IC also has an alert mechanism that can output an interrupt (INT) signal via the INT pin. The low-state INT pulse is output for 256μs to notify the system of operation changes. The INT output is designed as an open-drain structure that needs an external pull-up voltage source in real operation. The INT signal can be masked via REG18h and REG19h.

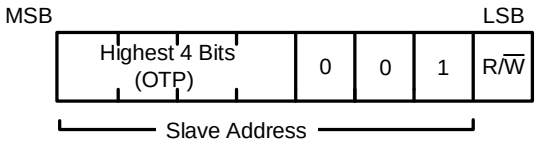
Address

To avoid having multiple devices on the same I²C bus with the same address, the MP2760's address can be configured via the one-time programmable (OTP) memory (OTP address).

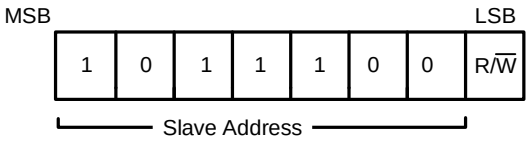
To support multiple MP2760 devices on the same I²C/SMBUS lines, the device OTP address can be adjusted via the REG05h, bits[6:3].

The MP2760 also has a universal address, 5Ch. When only one MP2760 device is in use, 5Ch or the OTP address can be used as the communication address.

The OTP address is 7 bits long, followed by the 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). REG05h, bits[6:3] can be configured via the OTP memory. Figure 14 shows the address bit arrangement for the OTP address and universal address (5Ch).



OTP Address



Universal Address (5Ch)

Figure 14: 7-Bit Address

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SMBus Alert Response Address (ARA)

The SMBus alert response address (ARA) is a special address that can be used by the bus host.

If more than one slave-only device is connected on the bus, and all the INT lines are connected, a slave-only device can signal to the host that is wants to talk via INT. The host processes the interrupt signal and simultaneously accesses all INT devices through the Alert Response Address (ARA). Only the devices that pulled INT low acknowledge the ARA.

The host performs a modified receive byte operation. The 7-bit device address transmitted by the slave is placed in the 7 most significant bits of the byte. The eighth bit can be a 0 or 1 to indicate a write or read, respectively.

The SMBus ARA is 0b0001 100.

Byte Format

Each byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Data is transferred with the most significant bit (MSB) first.

Each byte has to be followed by an acknowledge (ACK) bit, which is generated by the receiver, to signal to the transmitter that the byte was successfully received.

The ACK signal is defined as when the transmitter releases the SDA during the acknowledge clock pulse. Then the receiver pulls SDA low, and SDA stays low during the period of the ninth clock.

If SDA is high during the ninth clock, this is defined as the not acknowledge (NACK) signal. The master can then generate either a stop condition to abort the transfer or a repeated start (Sr) condition to start a new transfer.

All clock pulses, including the acknowledge pulse (ninth clock pulse), are generated by the master. If the register address is not defined, the IC sends back NACK and returns to an idle state.

Figure 16, Figure 17, and Figure 18 provide examples of different transmissions.

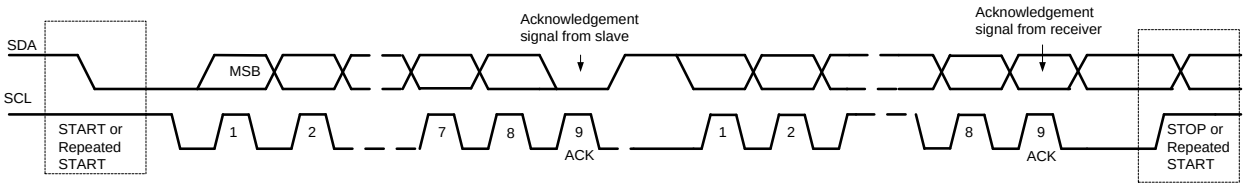

Figure 15: Acknowledge Bit

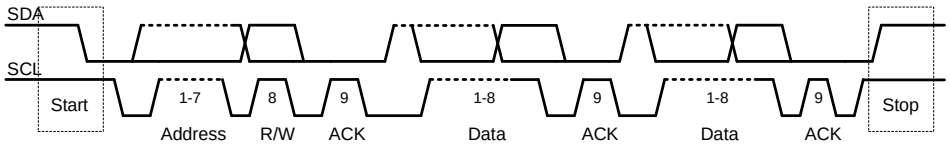

Figure 16: Byte Format

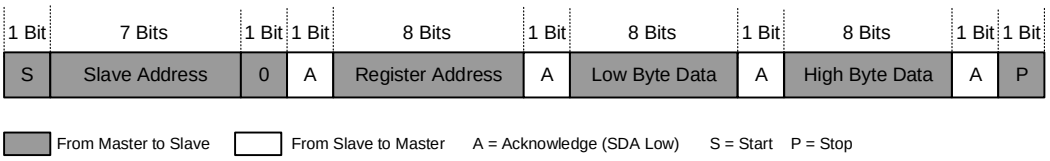

Figure 17: Singe Word Write

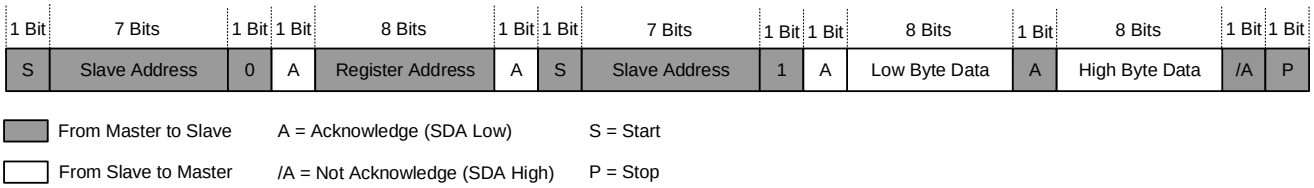

Figure 18: Single Word Read

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REGISTER MAP (6)

Register Name	Register Address	OTP (7)	R/W	Description
REG05h(6)	0x05	Yes	R/W	Sets the device address.
REG06h	0x06	Yes	R/W	Sets the minimum input voltage limit in charge mode.
REG07h	0x07	Yes	R/W	Sets the minimum system voltage.
REG08h	0x08	Yes	R/W	Sets the input current limit in charge mode.
REG09h	0x09	No	R/W	Sets the output voltage in source mode.
REG0Ah	0x0A	No	R/W	Sets the output current limit in source mode.
REG0Bh	0x0B	Yes	R/W	Sets the battery low voltage threshold and enables battery discharge current regulation in source mode.
REG0Ch	0x0C	No	R/W	Sets the JEITA action.
REG0Dh	0x0D	Yes	R/W	Sets temperature protections.
REG0Eh	0x0E	Yes	R/W	Configures register 0.
REG0Fh	0x0F	Yes	R/W	Configures register 1.
REG10h	0x10	Yes	R/W	Configures register 2.
REG11h	0x11	Yes	R/W	Configures register 3.
REG12h	0x12	Yes	R/W	Configures register 4.
REG14h	0x14	Yes	R/W	Sets the charge current
REG15h	0x15	Yes	R/W	Sets the battery-full voltage.
REG16h	0x16	No	R	Status and fault register 0.
REG17h	0x17	No	R	Status and fault register 1.
REG18h	0x18	No	R/W	INT mask setting register 0.
REG19h	0x19	No	R/W	INT mask setting register 1.
REG22h	0x22	No	R	Returns the internal DAC output of the input current limit.
REG23h	0x23	No	R	Returns the ADC input voltage result.
REG24h	0x24	No	R	Returns the ADC input current result.
REG25h	0x25	No	R	Returns the ADC battery voltage per cell result.
REG26h	0x26	No	R	Returns the ADC system voltage result.
REG27h	0x27	No	R	Returns the ADC battery charge current result.
REG28h	0x28	No	R	Returns the ADC NTC-sense voltage ratio result.
REG29h	0x29	No	R	Returns the ADC TS-sense voltage ratio result.
REG2Ah	0x2A	No	R	Returns the ADC junction temperature result.
REG2Bh	0x2B	No	R	Returns the ADC battery discharge current result.
REG2Ch	0x2C	No	R	Returns the ADC output voltage result in source mode.
REG2Dh	0x2D	No	R	Returns the ADC output current result in source mode.

Notes:

6) The default device OTP address is 69h, and the universal address is 5Ch. See the Address section on page 35.
7) OTP stands for one-time programmable (OTP) memory.

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REGISTER MAP (MP2760GVT-000A)

REG05h: Device Address Settings

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
[15:10]	RESERVED	0	N/A	N/A	Reserved.	Reserved.
9	WD_SET	1	No	R/W	0: Disabled 1: Enabled	When this bit is set to 0, the watchdog timer is disabled automatically when V_{IN} is absent.
8	TLOW_EN	0	No	R	0: Disabled (I^2C) 1: Enabled (SMBus)	Default: 0 (Disabled (I^2C)) To be compliant with SMBus, a 25ms timer must release SCL and SDA (reset the communication) if the timer expires. This bit can be configured via the OTP.
7	RESERVED	1	N	R	Reserved.	Reserved.
6	ADDR[3]	1	No	R		Default: 0b1101 These bits determine the highest 4 bits of the device's address. These bits can be configurable via the OTP.
5	ADDR[2]	1	No	R		
4	ADDR[1]	0	No	R		
3	ADDR[0]	1	No	R		
[2:1]	RESERVED	0	N/A	N/A	Reserved.	Reserved.
0	RESERVED	1	N/A	N/A	Reserved.	Reserved.

REG06h: Input Minimum Voltage Limit Settings

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
[15:8]	RESERVED	0	N/A	N/A	Reserved.	Reserved.
7	V_{IN_MIN}[7]	0	Yes	R/W	10240mV.	Default: 4.56V Range: Up to 20.4V These bits set the minimum input voltage limit. They can be configured via the OTP.
6	V_{IN_MIN}[6]	0	Yes	R/W	5120mV.	
5	V_{IN_MIN}[5]	1	Yes	R/W	2560mV.	
4	V_{IN_MIN}[4]	1	Yes	R/W	1280mV.	
3	V_{IN_MIN}[3]	1	Yes	R/W	640mV.	
2	V_{IN_MIN}[2]	0	Yes	R/W	320mV.	
1	V_{IN_MIN}[1]	0	Yes	R/W	160mV.	
0	V_{IN_MIN}[0]	1	Yes	R/W	80mV.	

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REG07h: System Minimum Voltage Settings

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
[15:9]	RESERVED	0	N/A	N/A	Reserved.	Reserved.
8	RESERVED	0	N/A	N/A	Internal use only.	Do not change this bit's value.
7	RESERVED	0	N/A	N/A	Internal use only.	Do not change this bit's value.
6	V_{SYS_MIN}[6]	0	Yes	R/W	12800mV.	Default: 6.4V (for 2 cells) Range: Up to 25.4V These bits set the absolute minimum system regulation voltage. They can be configured via the OTP. It is recommended to set these values to a different value according to battery cell count.
5	V_{SYS_MIN}[5]	1	Yes	R/W	6400mV.	
4	V_{SYS_MIN}[4]	0	Yes	R/W	3200mV.	
3	V_{SYS_MIN}[3]	0	Yes	R/W	1600mV.	
2	V_{SYS_MIN}[2]	0	Yes	R/W	800mV.	
1	V_{SYS_MIN}[1]	0	Yes	R/W	400mV.	
0	V_{SYS_MIN}[0]	0	Yes	R/W	200mV.	

REG08h: Input Current Limit Settings

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
[15:7]	RESERVED	0	N/A	N/A	Reserved.	Reserved.
6	I_{IN_LIM}[6]	0	Yes	R/W	3200mA.	Default: 500mA Range: Up to 5A These bits set the input current limit. These bits can be configured via the OTP. Note that when RS1 changes to 5mΩ, the internal gain should also be changed via REG10h, bit[8]. The LSB is unchanged.
5	I_{IN_LIM}[5]	0	Yes	R/W	1600mA.	
4	I_{IN_LIM}[4]	0	Yes	R/W	800mA.	
3	I_{IN_LIM}[3]	1	Yes	R/W	400mA.	
2	I_{IN_LIM}[2]	0	Yes	R/W	200mA.	
1	I_{IN_LIM}[1]	1	Yes	R/W	100mA.	
0	I_{IN_LIM}[0]	0	Yes	R/W	50mA.	

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REG09h: Output Voltage Settings in Source Mode

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
[15:12]	RESERVED	0	N/A	R/W	Reserved.	Reserved.
11	VIN_SRC_OS	0	No	R/W	0: 0V 1: 0.64V	This bit sets the voltage offset in source mode.
10	VIN_SRC_CFG	0	No	R/W	0: Configured via REG09h, bits[9:0] 1: Configured via the FB pin	This bit determines how the output voltage is configured in source mode. If this bet is set to 1, REG09h, bits[9:0] should be always set to 5V.
9	V_{IN_SRC}[9]	0	No	R/W	10240mV.	Default: 4.98V Range: Up to 20.46V These bits set the output voltage in source mode.
8	V_{IN_SRC}[8]	0	No	R/W	5120mV.	
7	V_{IN_SRC}[7]	1	No	R/W	2560mV.	
6	V_{IN_SRC}[6]	1	No	R/W	1280mV.	
5	V_{IN_SRC}[5]	1	No	R/W	640mV.	
4	V_{IN_SRC}[4]	1	No	R/W	320mV.	
3	V_{IN_SRC}[3]	1	No	R/W	160mV.	
2	V_{IN_SRC}[2]	0	No	R/W	80mV.	
1	V_{IN_SRC}[1]	0	No	R/W	40mV.	
0	V_{IN_SRC}[0]	1	No	R/W	20mV.	

REG0Ah: Battery Impedance Compensation and Output Current Limit Settings

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
[15:14]	RESERVED	0	N/A	N/A	Reserved.	Reserved.
13	BATTR[2]	0	Yes	R/W	200mΩ/cell.	Default: 0Ω/cell Range: 0Ω/cell to 350mΩ/cell These bits predict the input's battery internal impedance and cable impedance.
12	BATTR[1]	0	Yes	R/W	100mΩ/cell.	
11	BATTR[0]	0	Yes	R/W	50mΩ/cell.	
10	V_{CLAMP}[2]	0	Yes	R/W	240mV/cell.	Default: 0mV/cell Range: 0mV/cell to 420mV/cell These bits set the maximum compensation voltage, and should be added to original battery-full regulation voltage if the IR compensation function is used.
9	V_{CLAMP}[1]	0	Yes	R/W	120mV/cell.	
8	V_{CLAMP}[0]	0	Yes	R/W	60mV/cell.	
7	RESERVED	0	N/A	NA	Reserved.	Reserved.
6	I_{IN_SRC}[6]	0	Yes	R/W	3200mA.	Default: 2000mA Range: Up to 6350mA These bits set the output current limit in source mode. Note that when RS1 changes to 5mΩ, the internal gain should be changed via REG10h, bit[8]. The LSB remains unchanged.
5	I_{IN_SRC}[5]	1	Yes	R/W	1600mA.	
4	I_{IN_SRC}[4]	0	Yes	R/W	800mA.	
3	I_{IN_SRC}[3]	1	Yes	R/W	400mA.	
2	I_{IN_SRC}[2]	0	Yes	R/W	200mA.	
1	I_{IN_SRC}[1]	0	Yes	R/W	100mA.	
0	I_{IN_SRC}[0]	0	Yes	R/W	50mA.	

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REG0Bh: Battery Low Voltage Settings and Battery Discharge Current Regulation

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
[15:14]	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
13	VBATT_LOW_EN	1	Yes	R/W	0: Disabled 1: Enabled	Default: 1 (Enabled) This bit enables the battery low voltage protection. This bit can be configured via the OTP.
12	V_{BATT_PRE}	1	No	R/W	0: 2.5V/cell 1: 3.0V/cell	Default: 1 (3.0V/cell) This bit sets the pre-charge to linear CC charge threshold.
11	BATTLOW_ACT	0	Yes	R/W	0: Only generate INT signal 1: Generate INT signal and latch off the DC/DC converter	Default: 0 (Only generate INT signal) This bit determines the behavior for battery low voltage protection when REG0Bh, bit[13] is set to 1. When $V_{BATT} < V_{BATT_LOW}$, which is set via REG0Bh, bits[10:9], an INT signal is asserted to inform the host. The DC/DC converter can also be latched off. This bit can be configured via the OTP. Note that either charging the battery or toggling the DSCHG_EN bit clears the DSCHG_FLT bit. Then source mode can be enabled again. When source mode is disabled, the BATTLOW comparator does not operate.
10	V_{BATT_LOW}[1]	0	No	R/W	00: 3.0V/cell 01: 3.1V/cell 10: 3.2V/cell 11: 3.3V/cell	Default: 00 (3.0V/cell) These bits set the low battery voltage threshold for battery low voltage protection.
9	V_{BATT_LOW}[0]	0	No	R/W		
8	I_{BATT_DSCHG} EN	0	No	R/W	0: Disabled 1: Enabled	Default: 0 (Disabled) This bit enables battery discharge current regulation in source mode.
7	I_{BATT_DSCHG}[7]	1	No	R/W	6400mA.	Default: 6.4A Range: Up to 12.75A These bits set the battery discharge current in source mode.
6	I_{BATT_DSCHG}[6]	0	No	R/W	3200mA.	
5	I_{BATT_DSCHG}[5]	0	No	R/W	1600mA.	
4	I_{BATT_DSCHG}[4]	0	No	R/W	800mA.	
3	I_{BATT_DSCHG}[3]	0	No	R/W	400mA.	
2	I_{BATT_DSCHG}[2]	0	No	R/W	200mA.	
1	I_{BATT_DSCHG}[1]	0	No	R/W	100mA.	
0	I_{BATT_DSCHG}[0]	0	No	R/W	50mA.	

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REG0Ch: JEITA Action Settings

Bit	Name	Default	Reset by WTD	R/W	Description	Comment
15	RESERVED	0	N/A	N/A	Reserved.	Reserved.
14	WARM_ACT[1]	0	Yes	R/W	00: No action 01: Only reduce V_{BATT_REG} 10: Only reduce I_{CC} 11: Reduce both V_{BATT_REG} and I_{CC}	These bits determine the device's behavior if NTC warm protection occurs.
13	WARM_ACT[0]	1	Yes	R/W		
12	COOL_ACT[1]	1	Yes	R/W	00: No action 01: Only reduce V_{BATT_REG} 10: Only reduce I_{CC} 11: Reduce both V_{BATT_REG} and I_{CC}	These bits determine the device's behavior if NTC cool protection occurs.
11	COOL_ACT[0]	0	Yes	R/W		
10	JEITA_VSET[4]	1	Yes	R/W	320mV/cell.	Default: 320mV/cell Range: Up to 620mV/cell These bits set the decrease value for the battery-full voltage if NTC cool or warm protection occur. The battery-full voltage can be set via REG15h.
9	JEITA_VSET[3]	0	Yes	R/W	160mV/cell.	
8	JEITA_VSET[2]	0	Yes	R/W	80mV/cell.	
7	JEITA_VSET[1]	0	Yes	R/W	40mV/cell.	
6	JEITA_VSET[0]	0	Yes	R/W	20mV/cell.	
5	JEITA_ISET[1]	0	Yes	R/W	00: 1/2 times 01: 1/4 times 10: 1/8 times 11: 1/16 times	Default: 01 (1/4 times) These bits set the scaling value of the constant current charge current. The constant current charge current can be set via REG14h.
4	JEITA_ISET[0]	1	Yes	R/W		
[3:0]	RESERVED	0	N/A	N/A	Reserved.	Reserved.

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REG0Dh: Temperature Protection Settings

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15	TS_EN	1	No	R/W	0: Disabled 1: Enabled	Default: 1 (Enabled) This bit enables the external temperature sense function.
14	TS_ OPTION	1	Yes	R/W	0: Input connector 1: BATFET	Default: 1 (BATFET) This bit determines where the temperature is sensed. This bit can be configured via the OTP.
13	TS_ACT	1	Yes	R/W	0: Only deliver INT signal after reaching TS threshold 1: Deliver INT signal and take TS action	Default: 1 (Deliver INT signal and take TS action) This bit determines the behavior if TS over-temperature protection (OTP) occurs. An INT signal is asserted after TS OTP, and charge current or input current regulation can be implemented. This bit can be configured via the OTP.
12	V_{TS_HOT}[2]	1	No	R/W	000: 9% (100°C) 001: 10% (95°C) 010: 11.3% (90°C) 011: 12.7% (85°C) 100: 14.3% (80°C) 101: 16.1% (75°C) 110: 18.2% (70°C) 111: 20.6% (65°C)	Default: 100 (14.3% (80°C)) These bits configure the TS OTP threshold as a percentage of V_{NTC}. Assume that the thermistor is 103AT, with a 10kΩ pull-up resistor.
11	V_{TS_HOT}[1]	0	No	R/W		
10	V_{TS_HOT}[0]	0	No	R/W		
9	NTC_EN	1	No	R/W	0: Disabled 1: Enabled	Default: 1 (Enabled) This bit enables NTC protection.
8	NTC_ACT	1	Yes	R/W	0: Only deliver INT signal after reaching NTC threshold 1: Deliver INT and take JEITA action	Default: 1 (Deliver INT and take JEITA action) This bit determines the behavior if NTC protection occurs. An INT signal is asserted, and additional actions can be taken. This bit can be configured via the OTP.
7	V_{HOT}[1]	1	No	R/W	00: 29.1% (50°C) 01: 25.9% (55°C) 10: 23.0% (60°C) 11: 20.4% (65°C)	Default: 10 (23.0% (60°C)) These bits set the NTC hot temperature threshold (as a percentage of V_{NTC}). Assume that the thermistor is 103AT.
6	V_{HOT}[0]	0	No	R/W		
5	V_{WARM}[1]	0	No	R/W	00: 36.5% (40°C) 01: 32.6% (45°C) 10: 29.1% (50°C) 11: 25.9% (55°C)	Default: 01 (32.6% (45°C)) These bits set the NTC warm temperature threshold (as a percentage of V_{NTC}). Assume that the thermistor is 103AT.
4	V_{WARM}[0]	1	No	R/W		
3	V_{COOL}[1]	1	No	R/W	00: 74.2% (0°C) 01: 69.6% (5°C) 10: 64.8% (10°C) 11: 59.9% (15°C)	Default: 10 (64.8% (10°C)) These bits set the NTC cool temperature threshold (as a percentage of V_{NTC}). that the thermistor is 103AT.
2	V_{COOL}[0]	0	No	R/W		
1	V_{COLD}[1]	0	No	R/W	00: 78.4% (-5°C) 01: 74.2% (0°C) 10: 69.6% (5°C) 11: 64.8% (10°C)	Default: 01 (74.2% (0°C)) These bits set the NTC cold temperature threshold (as a percentage of V_{NTC}). Assume that the thermistor is 103AT.
0	V_{COLD}[0]	1	No	R/W		

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REG0Eh: Configuration Register 0

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
[15:9]	RESERVED	0	N/A	N/A	Reserved.	Reserved.
8	ADC_START	0	No	R/W	0: Disable ADC 1: Enable ADC	This bit enables the ADC when it is set to one-shot conversion mode via REG0Eh, bit[7]. In this mode, the bit returns to 0 after conversion is complete. When the DC/DC converter is enabled, this bit is always 1 to enable the ADC. This bit is read-only when ADC_CONV = 1. The bit stays high during ADC conversion.
7	ADC_CONV	0	No	R/W	0: One-shot conversion 1: Continuous conversion	This bit determines the behavior for ADC conversion.
6	SW_FREQ[2]	0	Yes	R/W	000: 500kHz 001: 600kHz 010: 700kHz 011: 800kHz 100: 750kHz 101: 900kHz 110: 1000kHz 111: 1200kHz	Default: 001 (600kHz) These bits set the buck-boost converter's switching frequency. This bit can be configured via the OTP.
5	SW_FREQ[1]	0	Yes	R/W		
4	SW_FREQ[0]	1	Yes	R/W		
[3:0]	RESERVED	0	N/A	N/A	Internal use only.	Do not change this bit's value.

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REG0Fh: Configuration Register 1

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15	TJ_REG_EN	1	Yes	R/W	0: Disabled 1: Enabled	Default: 1 (Enabled) Enables junction over-temperature regulation. Can be configured via the OTP.
14	T_{J_REG}[2]	1	Yes	R/W	000: 80°C 001: 90°C 010: 95°C 011: 100°C 100: 105°C 101: 110°C 110: 115°C 111: 120°C	Default: 111 (120°C) These bits set the junction temperature regulation point.
13	T_{J_REG}[1]	1	Yes	R/W		
12	T_{J_REG}[0]	1	Yes	R/W		
11	I_{TC}[3]	0	Yes	R/W	400mA.	Default: 100mA Range: Up to 750mA These bits set the trickle-charge current. They can be configured via the OTP.
10	I_{TC}[2]	0	Yes	R/W	200mA.	
9	I_{TC}[1]	1	Yes	R/W	100mA.	
8	I_{TC}[0]	0	Yes	R/W	50mA.	
7	I_{PRE}[7]	0	Yes	R/W	800mA.	Default: 400mA Range: Up to 1.5A These bits set the pre-charge current. They can be configured via the OTP.
6	I_{PRE}[6]	1	Yes	R/W	400mA.	
5	I_{PRE}[5]	0	Yes	R/W	200mA.	
4	I_{PRE}[4]	0	Yes	R/W	100mA.	
3	I_{TERM}[3]	0	Yes	R/W	400mA.	Default: 200mA Range: Up to 750mA These bits set the termination current. They can be configured via the OTP.
2	I_{TERM}[2]	1	Yes	R/W	200mA.	
1	I_{TERM}[1]	0	Yes	R/W	100mA.	
0	I_{TERM}[0]	0	Yes	R/W	50mA.	

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REG10h: Configuration Register 2

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15	RESERVED	0	NA	N/A	Reserved.	Reserved.
14	ACGATE_ CTRL	0	No	R/W	0: Do not force ACGATE on 1: Force ACGATE on	Default: 0 (Do not force ACGATE on) This bit controls ACGATE. It can force ACGATE to turn on the external MOSFET when it is set to 1. The ACGATE state depends on the ADP voltage.
13	BGATE_ CTRL	0	No	R/W	0: Do not force BGATE off 1: Force BGATE off	Default: 0 (Do not force BGATE off) This bit controls BGATE. It can force BGATE to turn off the external MOSFET when it is set to 1. The BGATE state depends on the BGATE control logic in NVDC mode.
12	TS/IMON	0	Yes	R/W	0: TS/IMON acts as TS 1: TS/IMON acts as IMON	Default: 0 (TS/IMON acts as TS) This bit configures the TS/IMON function. This bit can be configured via the OTP.
11	VRECH	1	Yes	R/W	0: -100mV/cell 1: -200mV/cell	Default: 1 (-200mV/cell) This bit sets the automatic recharge threshold when compared to the battery-full voltage. This bit can be configured via the OTP.
10	BAT_NUM[1]	0	Yes	R/W	00: 1-cell 01: 2-cell 10: 3-cell 11: 4-cell	Default: 01 (2-cell) This bit sets the battery cells in series. This bit can be configured via the OTP.
9	BAT_NUM[0]	1	Yes	R/W		
8	IN_RSNS	0	Yes	R/W	0: 10mΩ 1: 5mΩ	This bit sets the input current sense gain. The gain should be set according to the external sense resistor (RS1). A 10mΩ sense FET is assumed to be the default. This bit can be configured via the OTP.
7	IBATT_ RSNS	0	Yes	R/W	0: 10mΩ 1: 5mΩ	This bit sets the battery current sense gain. The gain should be set according to the external sense resistor (RS2). A 10mΩ sense FET is assumed to be the default. This bit can be configured via the OTP.
6	ACGATE_ EN	1	No	R/W	0: Disabled 1: Enabled	Default: 1 (Enabled) This bit enables the ACGATE driver. It's enabled by default.
5	RESERVED	1	N/A	R/W	Internal use only.	Do not change this bit's value.
4	V_{TRACK}[4]	1	Yes	R/W	80mV/cell.	Default: 100mV/cell Range: Up to 155mV/cell These bits set the track voltage in NVDC power path management control. The minimum system voltage ($V_{SYS_MIN_REG}$) is regulated at V_{SYS_MIN} + (V_{TRACK} x BAT_NUM). These bits can be configured via the OTP.
3	V_{TRACK}[3]	0	Yes	R/W	40mV/cell.	
2	V_{TRACK}[2]	1	Yes	R/W	20mV/cell.	
1	V_{TRACK}[1]	0	Yes	R/W	10mV/cell.	
0	V_{TRACK}[0]	0	Yes	R/W	5mV/cell.	

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REG11h: Configuration Register 3

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15	RESERVED	0	N/A	N/A	Reserved.	Reserved.
14	V_{SYS_OV}[1]	1	No	R/W	00: 106% 01: 120% 10: 115% 11: 110%	Default: 11 (110%) These bits set the system (SYS) over-voltage (OV) threshold (as a percentage of the system regulation voltage). This value is also used as the output OV threshold in source mode.
13	V_{SYS_OV}[0]	1	No	R/W		
12	V_{SYS_UV}[1]	0	No	R/W	00: 75% 01: 80% 10: 85% 11: 30%	These bits sets the system under-voltage threshold which is as percentage of system regulation voltage. It has a 75% default. This is also reused for output under-voltage threshold in source mode
11	V_{SYS_UV}[0]	0	No	R/W		
10	$V_{IN_OVP_DGL}$	0	No	R/W	0: 1µs 1: 15ms	Default: 0 (1µs) This bit sets the deglitch time for input over-voltage protection (OVP).
9	V_{IN_UVLO}[1]	0	Yes	R/W	00: 3.2V 01: 6.4V 10: 12V 11: 16.8V	Default: 00 (3.2V) These bits sets the input under-voltage protection (UVP) threshold. These bits can be configured via the OTP.
8	V_{IN_UVLO}[0]	0	Yes	R/W		
7	V_{IN_OVP}[1]	1	Yes	R/W	00: 7.2V 01: 11.2V 10: 17.6V 11: 22.4V	Default: 11 (22.4V) These bits are used to set the input OVP threshold. These bits can be configured via the OTP.
6	V_{IN_OVP}[0]	1	Yes	R/W		
5	SYSOVP_EN	1	No	R/W	0: Disabled 1: Enabled	Default: 1 (Enabled) This bit is enables SYS OVP.
4	RESERVED	0	N/A	NA	Internal use only.	Do not change this bit's value.
3	BATTOVP_EN	1	No	R/W	0: Disabled 1: Enabled	Default: 1 (Enabled) This bit enables battery (BATT) OVP.
2	RESERVED	0	N/A	N/A	Internal use only.	Do not change this bit's value.
1	RESERVED	0	N/A	N/A	Internal use only.	Do not change this bit's value.
0	RESERVED	0	N/A	R/W	Internal use only.	Do not change this bit's value.

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REG12h: Configuration Register 4

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15	RESERVED	0	N/A	N/A	Internal use only.	Do not change this bit's value.
14	RESERVED	0	N/A	N/A	Internal use only.	Do not change this bit's value.
13	TMR_EN	1	Yes	R/W	0: Disabled 1: Enabled	Default: 1 (Enabled) This bit enables the charging safety timer (both the linear charge timer and switching CC/CV charge timer). This bit can be configured via the OTP.
12	CHG_TMR[1]	1	Yes	R/W	00: 5 hours 01: 8 hours 10: 12 hours 11: 20 hours	Default: 11 (20 hours) These bits set the fast-charge timer.
11	CHG_TMR[0]	1	Yes	R/W		
10	TMR2X_EN	1	Yes	R/W	0: The safety timer is not doubled during input DPM or thermal regulation. 1: The safety timer is doubled during input DMP and thermal regulation.	This bit sets the safety timer during DPM and thermal regulation. It is set to 1 by default.
9	WTD_RST	0	Yes	R/W	0: Normal 1: Reset	Default: 0 (Normal) This bit resets the I²C watchdog timer, and returns to 0 after the after timer is reset.
8	WTD[1]	0	Yes	R/W	00: Timer disabled 01: 40s 10: 80s 11: 175s	Default: 00 (Timer disabled) This bit sets the I²C watchdog timer. This bit can be configured via the OTP.
7	WTD[0]	0	Yes	R/W		
6	DC/DC_EN	1	Yes	R/W	0: Disabled 1: Enabled	Default: 1 (Enabled) This bit enables the DC/DC converter. This bit can be configured via the OTP.
5	BGATE_EN	1	Yes	R/W	0: Disabled 1: Enabled	Default: 1 (Enabled) This bit enables the BGATE driver. When disabled, the BGATE output stays in a Hi-Z state. This bit can be configured via the OTP.
4	TERM_EN	1	Yes	R/W	0: Disabled 1: Enabled	This bit enables charge termination.
3	SRC_EN	0	Yes	R/W	0: Disable source mode 1: Enable source mode	This bit is used to enable source mode configuration. It is set to 0 by default. SRC_EN will over-ride charge enable function.
2	REG_RST	0	Yes	R/W	0: Keep current register setting 1: Reset to the default register value and reset the safety timer	Default: 0 (Keep current register setting) This bit resets the register. It resets to 0 after the register is reset.

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1	IINLIM_EN	1	Yes	R/W	0: Disabled 1: Enabled	Default: 1 (Enabled) This bit enables the input current limit loop (IIN_LIM). It is set to 1 by default.
0	CHG_EN	1	Yes	R/W	0: Charge disabled (only turn off BATFET) 1: Charge enabled	Default: 1 (Charge enabled) This bit configures the charge mode. SRC_EN overrides the CHG_EN enable function. This bit can be configured via the OTP.

REG14h: Charge Current Setting

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
[15:14]	RESERVED	0	N/A	N/A	Reserved.	Reserved.
13	I_{CC}[7]	0	Yes	R/W	6400mA.	Default: 2A Offset: 0A Range: Up to 6A These bits set the charge current. These bits can be configured via the OTP.
12	I_{CC}[6]	0	Yes	R/W	3200mA.	
11	I_{CC}[5]	1	Yes	R/W	1600mA.	
10	I_{CC}[4]	0	Yes	R/W	800mA.	
9	I_{CC}[3]	1	Yes	R/W	400mA.	
8	I_{CC}[2]	0	Yes	R/W	200mA.	
7	I_{CC}[1]	0	Yes	R/W	100mA.	
6	I_{CC}[0]	0	Yes	R/W	50mA.	
[5:0]	RESERVED	0	N/A	N/A	Reserved.	Reserved.

REG15h: Battery-Full Voltage Setting

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15	RESERVED	0	N/A	N/A	Reserved.	Reserved.
14	V_{BATT_REG}[10]	0	Yes	R/W	10240mV.	Default: 8.4V Range: 3.4V/cell to 4.68V/cell (for different cell counts) These bits set the charge-full voltage. These bits can be configured via the OTP.
13	V_{BATT_REG}[9]	1	Yes	R/W	5120mV.	
12	V_{BATT_REG}[8]	1	Yes	R/W	2560mV.	
11	V_{BATT_REG}[7]	0	Yes	R/W	1280mV.	
10	V_{BATT_REG}[6]	1	Yes	R/W	640mV.	
9	V_{BATT_REG}[5]	0	Yes	R/W	320mV.	
8	V_{BATT_REG}[4]	0	Yes	R/W	160mV.	
7	V_{BATT_REG}[3]	1	Yes	R/W	80mV.	
6	V_{BATT_REG}[2]	0	Yes	R/W	40mV.	
5	V_{BATT_REG}[1]	0	Yes	R/W	20mV.	
4	V_{BATT_REG}[0]	0	Yes	R/W	10mV.	
[3:0]	RESERVED	0	N/A	R/W	Reserved.	Reserved.

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REG16h: Status and Fault Register 0

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15	MD_STAT[1]	0	No	R	00/10: Standby 01/11: Operation mode	These bits indicate the DC/DC operation status. The device asserts an INT signal when the state changes.
14	MD_STAT[0]	0	No	R		
13	PG_STAT	0	No	R	0: V_{IN} not power good 1: V_{IN} power good	Default: 0 (V_{IN} not power good) This bit indicates the power good status. The device asserts an INT signal when this bit changes from 0 to 1.
12	SWITCH_ STAT[1]	0	No	R	00: Idle 01: Buck 10: Buck-boost 11: Boost	Default: 00 (Idle) These bits indicate the DC/DC operation mode.
11	SWITCH_ STAT[0]	0	No	R		
10	BATT_ MISS_STAT	0	No	R	0: Normal 1: Battery missing	Default: 0 (Normal) This bit indicates if the battery is missing. It asserts INT when this bit changes from 0 to 1.
9	RESERVED	0	No	R	Reserved.	Reserved.
8	CHG_ STAT[2]	0	No	R	000: No charging 001: Trickle charge 010: Pre-charge 011: CC charge 100: CV charge 101: Charge termination	Default: 000 (No charging) These bits indicate the charging status. The device asserts an INT signal when the state changes.
7	CHG_ STAT[1]	0	No	R		
6	CHG_ STAT[0]	0	No	R		
5	VIN_MIN_ STAT	0	No	R	0: Not in the input voltage limit loop 1: In the input voltage limit	Default: 0 (Not in the input voltage limit loop) This bit indicates whether the MP2760 stays in the input voltage loop. The device asserts an INT signal when this bit changes from 0 to 1.
4	IIN_LIM_ STAT	0	No	R	0: Not in the input current limit loop 1: In the input current limit loop	Default: 0 (Not in the input current limit loop) This bit indicates whether the MP2760 stays in the input current loop. The device asserts an INT signal when this bit changes from 0 to 1.
3	RESERVED	0	No	R	Reserved	Reserved
2	BATFET_ OC	0	No	R	0: Normal operation 1: A BATFET over-current (OC) condition has occurred	Default: 0 (Normal) This bit indicates whether the discharge current threshold exceeds the current threshold. The device asserts an INT signal when the BATFET OC happens.

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1	TS_FAULT	0	No	R	0: Normal operation 1: A TS hot condition has occurred	This bit indicates whether a TS related fault happens. The device asserts an INT signal when the TS hot happens .
0	RESERVED	0	No	R	Reserved.	Reserved.

REG17h: Status and Fault Register 1

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15	VIN_ SRC_OV	0	No	R	0: Normal operation 1: Output OVP in source mode	This bit indicates whether output over-voltage protection (OVP) occurs in source mode. It asserts an INT signal when output OVP occurs.
14	VIN_ SRC_UV	0	No	R	0: Normal operation 1: Output UVP in source mode	This bit indicates whether output under-voltage protection (UVP) occurs in source mode. It asserts an INT signal when the output UVP occurs.
13	VIN_ CHG_OV	0	No	R	0: Normal operation 1: Input OVP in charge mode	This bit indicates whether input OVP occurs in charging mode. It asserts an INT signal when input OVP occurs.
12	VADP_OV	0	No	R	0: Normal operation 1: VADP OVP	This bit indicates whether ADP OVP occurs in charging mode. It asserts an INT signal when VADP OVP occurs.
11	VSYS_OV	0	No	R	0: Normal operation 1: SYS OV	This bit indicates whether system OVP occurs in charging mode. It asserts an INT signal when SYS OVP occurs.
10	VSYS_UV	0	No	R	0: Normal operation 1: SYS UV	This bit indicates whether system UVP occurs in charging mode. It asserts an INT signal when the SYS UV occurs.
9	RESERVED	0	No	R	Reserved.	Reserved.
8	VBATT_OV	0	No	R	0: Normal operation 1: Battery OVP	This bit indicates whether battery OVP occurs in charging mode. It asserts an INT signal when battery OVP occurs.
7	VBATT_ LOW	0	No	R	0: Normal operation 1: Discharge stop due to BATT_LOW	This bit indicates whether there is a low battery voltage in source mode. It asserts an INT signal when BATT_LOW occurs.
6	WTD_EXP	0	No	R	0: Normal operation 1: Watchdog timer expiration	This bit indicates whether the watchdog timer expires.
5	CHG_TMR_ EXP	0	No	R	0: Normal operation 1: Charge Safety timer expiration	This bit indicates whether the charge safety timer has expired. It asserts an INT signal when the timer expires.

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4	THERM_ SHDN	0	No	R	0: Normal operation 1: Thermal Shutdown		This bit indicates if thermal shutdown occurs. It asserts an INT signal when the thermal shutdown happens.
3	RESERVED	0	N/A	R/W	Reserved.		Reserved.
2	NTC_ FAULT[2]	0	No	R	Charge mode: 000: Normal 001: NTC cold 010: NTC cool 011: NTC warm 100: NTC hot 111: NTC float	Source mode: 000: Normal 001: NTC cold 100: NTC hot 111: NTC float	These bits indicate if an NTC fault occurs in charging mode. It asserts an INT signal when fault happens.
1	NTC_ FAULT[1]	0	No	R			
0	NTC_ FAULT[0]	0	No	R			

REG18h: INT Mask Setting Register 0

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
15	RESERVED	0	Yes	R/W	Reserved.	For any fault that is masked, INT will not assert if the fault occurs. However, the fault bit is set.
14	VSYS_ FAULT	0	Yes	R/W	0: Masked 1: Not masked	
13	VIN_SRC_ FAULT	0	Yes	R/W	0: Masked 1: Not masked	
12	VIN_CHG OV_FAULT	0	Yes	R/W	0: Masked 1: Not masked	
11	PG_STAT	0	Yes	R/W	0: Masked 1: Not masked	
10	BATT_OV_ FAULT	0	Yes	R/W	0: Masked 1: Not masked	
9	BFET_OC	0	Yes	R/W	0: Masked 1: Not masked	
8	WTD_ FAULT	0	Yes	R/W	0: Masked 1: Not masked	
7	BATT_ LOW_ FAULT	0	Yes	R/W	0: Masked 1: Not masked	
6	BATT_ MISS_STAT	0	Yes	R/W	0: Masked 1: Not masked	
5	THERM_ SHDN	0	Yes	R/W	0: Masked 1: Not masked	
4	TS_FAULT	0	Yes	R/W	0: Masked 1: Not masked	
3	NTC_ FAULT	0	Yes	R/W	0: Masked 1: Not masked	
2	CHG_TMR_ FAULT	0	Yes	R/W	0: Masked 1: Not masked	
1	MD_STAT	0	Yes	R/W	0: Masked 1: Not masked	
0	CHG_STAT	0	Yes	R/W	0: Masked 1: Not masked	

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REG19h: INT Mask Setting Register 1

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
[15:2]	RESERVED	0	N/A	N/A	Reserved.	Reserved.
1	VIN_MIN_ STAT	0	Yes	R/W	0: Masked 1: Not masked	For any fault that is masked, the INT will not assert if the fault occurs. However, the fault bit is set.
0	IIN_LIM_ STAT	0	Yes	R/W	0: Masked 1: Not masked	

REG22h: Internal DAC Output of the Input Current Limit

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
[15:7]	RESERVED	0	N/A	NA	Reserved.	Reserved.
6	I_{IN_DPM}[6]	0	No	R	3200mA.	Default: 500mA These bits only indicate the real input current limit value, which is read-only.
5	I_{IN_DPM}[5]	0	No	R	1600mA.	
4	I_{IN_DPM}[4]	0	No	R	800mA.	
3	I_{IN_DPM}[3]	0	No	R	400mA.	
2	I_{IN_DPM}[2]	0	No	R	200mA.	
1	I_{IN_DPM}[1]	0	No	R	100mA.	
0	I_{IN_DPM}[0]	0	No	R	50mA.	

REG23h: ADC Result of the Input Voltage

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
[15:10]	Reserved	N/A	N/A	N/A	Reserved.	Reserved.
9	V_{IN_ADC}[9]	N/A	N/A	R	10240mV.	These bits indicate the result of the ADC conversion for the input voltage.
8	V_{IN_ADC}[8]	N/A	N/A	R	5120mV.	
7	V_{IN_ADC}[7]	N/A	N/A	R	2560mV.	
6	V_{IN_ADC}[6]	N/A	N/A	R	1280mV.	
5	V_{IN_ADC}[5]	N/A	N/A	R	640mV.	
4	V_{IN_ADC}[4]	N/A	N/A	R	320mV.	
3	V_{IN_ADC}[3]	N/A	N/A	R	160mV.	
2	V_{IN_ADC}[2]	N/A	N/A	R	80mV.	
1	V_{IN_ADC}[1]	N/A	N/A	R	40mV.	
0	V_{IN_ADC}[0]	N/A	N/A	R	20mV.	

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REG24h: ADC Result of the Input Current

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
[15:10]	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	I_{IN_ADC}[9]	N/A	N/A	R	3200mA.	These bits indicate the result of the ADC conversion for the input current.
8	I_{IN_ADC}[8]	N/A	N/A	R	1600mA.	
7	I_{IN_ADC}[7]	N/A	N/A	R	800mA.	
6	I_{IN_ADC}[6]	N/A	N/A	R	400mA.	
5	I_{IN_ADC}[5]	N/A	N/A	R	200mA.	
4	I_{IN_ADC}[4]	N/A	N/A	R	100mA.	
3	I_{IN_ADC}[3]	N/A	N/A	R	50mA.	
2	I_{IN_ADC}[2]	N/A	N/A	R	25mA.	
1	I_{IN_ADC}[1]	N/A	N/A	R	12.5mA.	
0	I_{IN_ADC}[0]	N/A	N/A	R	6.25mA.	

REG25h: ADC Result of the Battery Voltage per Cell

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
[15:10]	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	V_{BATT_ADC}[9]	N/A	N/A	R	2560mV/cell.	These bits indicate the ADC conversion of the battery voltage per cell. The real battery voltage should be the value read times cell numbers.
8	V_{BATT_ADC}[8]	N/A	N/A	R	1280mV/cell.	
7	V_{BATT_ADC}[7]	N/A	N/A	R	640mV/cell.	
6	V_{BATT_ADC}[6]	N/A	N/A	R	320mV/cell.	
5	V_{BATT_ADC}[5]	N/A	N/A	R	160mV/cell.	
4	V_{BATT_ADC}[4]	N/A	N/A	R	80mV/cell.	
3	V_{BATT_ADC}[3]	N/A	N/A	R	40mV/cell.	
2	V_{BATT_ADC}[2]	N/A	N/A	R	20mV/cell.	
1	V_{BATT_ADC}[1]	N/A	N/A	R	10mV/cell.	
0	V_{BATT_ADC}[0]	N/A	N/A	R	5mV/cell.	

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REG26h: ADC Result of the System Voltage

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
[15:10]	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	V_{SYS_ADC}[9]	N/A	N/A	R	10240mV.	These bits indicate the result of the ADC conversion for the system voltage.
8	V_{SYS_ADC}[8]	N/A	N/A	R	5120mV.	
7	V_{SYS_ADC}[7]	N/A	N/A	R	2560mV.	
6	V_{SYS_ADC}[6]	N/A	N/A	R	1280mV.	
5	V_{SYS_ADC}[5]	N/A	N/A	R	640mV.	
4	V_{SYS_ADC}[4]	N/A	N/A	R	320mV.	
3	V_{SYS_ADC}[3]	N/A	N/A	R	160mV.	
2	V_{SYS_ADC}[2]	N/A	N/A	R	80mV.	
1	V_{SYS_ADC}[1]	N/A	N/A	R	40mV.	
0	V_{SYS_ADC}[0]	N/A	N/A	R	20mV.	

REG27h: ADC Result of the Battery Charge Current

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
[15:10]	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	I_{BATT_ADC}[9]	N/A	N/A	R	6400mA.	These bits indicate the result of the ADC conversion for the charge current.
8	I_{BATT_ADC}[8]	N/A	N/A	R	3200mA.	
7	I_{BATT_ADC}[7]	N/A	N/A	R	1600mA.	
6	I_{BATT_ADC}[6]	N/A	N/A	R	800mA.	
5	I_{BATT_ADC}[5]	N/A	N/A	R	400mA.	
4	I_{BATT_ADC}[4]	N/A	N/A	R	200mA.	
3	I_{BATT_ADC}[3]	N/A	N/A	R	100mA.	
2	I_{BATT_ADC}[2]	N/A	N/A	R	50mA.	
1	I_{BATT_ADC}[1]	N/A	N/A	R	25mA.	
0	I_{BATT_ADC}[0]	N/A	N/A	R	12.5mA.	

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REG28h: ADC Result of the NTC-Sense Voltage Ratio

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
[15:10]	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	$NTC_{_ADC}[9]$	N/A	N/A	R	512/1024.	These bits indicate the ADC conversion of NTC voltage percentage of VNTC. The real battery temperature can be recalculated according to external divider and thermistor datasheet.
8	$NTC_{_ADC}[8]$	N/A	N/A	R	256/1024.	
7	$NTC_{_ADC}[7]$	N/A	N/A	R	128/1024.	
6	$NTC_{_ADC}[6]$	N/A	N/A	R	64/1024.	
5	$NTC_{_ADC}[5]$	N/A	N/A	R	32/1024.	
4	$NTC_{_ADC}[4]$	N/A	N/A	R	16/1024.	
3	$NTC_{_ADC}[3]$	N/A	N/A	R	8/1024.	
2	$NTC_{_ADC}[2]$	N/A	N/A	R	4/1024.	
1	$NTC_{_ADC}[1]$	N/A	N/A	R	2/1024.	
0	$NTC_{_ADC}[0]$	N/A	N/A	R	1/1024.	

REG29h: ADC Result of the TS-Sense Voltage Ratio

Bits	Name	Default	Reset by WTD	R/W	Description	Comment
[15:10]	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	$TS_{_ADC}[9]$	N/A	N/A	R	512/1024.	These bits indicate the ADC conversion of TS voltage percentage of VNTC.
8	$TS_{_ADC}[8]$	N/A	N/A	R	256/1024.	
7	$TS_{_ADC}[7]$	N/A	N/A	R	128/1024.	
6	$TS_{_ADC}[6]$	N/A	N/A	R	64/1024.	
5	$TS_{_ADC}[5]$	N/A	N/A	R	32/1024.	
4	$TS_{_ADC}[4]$	N/A	N/A	R	16/1024.	
3	$TS_{_ADC}[3]$	N/A	N/A	R	8/1024.	
2	$TS_{_ADC}[2]$	N/A	N/A	R	4/1024.	
1	$TS_{_ADC}[1]$	N/A	N/A	R	2/1024.	
0	$TS_{_ADC}[0]$	N/A	N/A	R	1/1024.	

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REG2Ah: ADC Result of the Junction Temperature

Bit	Name	Default	Reset by WTD	R/W	Description	Comment
[15:10]	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	TJ_{ADC}[9]	N/A	N/A	R	512.	These bits indicate the result of the ADC conversion for the junction temperature (T_J). T_J can be calculated with the following equation: T_J = 314 - 0.5703 x REG2Ah, bits[9:0]
8	TJ_{ADC}[8]	N/A	N/A	R	256.	
7	TJ_{ADC}[7]	N/A	N/A	R	128.	
6	TJ_{ADC}[6]	N/A	N/A	R	64.	
5	TJ_{ADC}[5]	N/A	N/A	R	32.	
4	TJ_{ADC}[4]	N/A	N/A	R	16.	
3	TJ_{ADC}[3]	N/A	N/A	R	8.	
2	TJ_{ADC}[2]	N/A	N/A	R	4.	
1	TJ_{ADC}[1]	N/A	N/A	R	2.	
0	TJ_{ADC}[0]	N/A	N/A	R	1.	

REG2Bh: ADC Result of the Battery Discharge Current in Source Mode

Bit	Name	Default	Reset by WTD	R/W	Description	Comment
[15:10]	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	$I_{BATT_DIS_ADC}$[9]	N/A	N/A	R	6400mA.	These bits indicate the result of the ADC conversion for the battery discharge current.
8	$I_{BATT_DIS_ADC}$[8]	N/A	N/A	R	3200mA.	
7	$I_{BATT_DIS_ADC}$[7]	N/A	N/A	R	1600mA.	
6	$I_{BATT_DIS_ADC}$[6]	N/A	N/A	R	800mA.	
5	$I_{BATT_DIS_ADC}$[5]	N/A	N/A	R	400mA.	
4	$I_{BATT_DIS_ADC}$[4]	N/A	N/A	R	200mA.	
3	$I_{BATT_DIS_ADC}$[3]	N/A	N/A	R	100mA.	
2	$I_{BATT_DIS_ADC}$[2]	N/A	N/A	R	50mA.	
1	$I_{BATT_DIS_ADC}$[1]	N/A	N/A	R	25mA.	
0	$I_{BATT_DIS_ADC}$[0]	N/A	N/A	R	12.5mA.	

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REG2Ch: ADC Result of the Output Voltage in Source Mode

Bit	Name	Default	Reset by WTD	R/W	Description	Comment
[15:10]	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	$V_{IN_SRC_ADC}$[9]	N/A	N/A	R	10240mV.	These bits indicate the ADC conversion of the output voltage at IN pin in source mode
8	$V_{IN_SRC_ADC}$[8]	N/A	N/A	R	5120mV.	
7	$V_{IN_SRC_ADC}$[7]	N/A	N/A	R	2560mV.	
6	$V_{IN_SRC_ADC}$[6]	N/A	N/A	R	1280mV.	
5	$V_{IN_SRC_ADC}$[5]	N/A	N/A	R	640mV.	
4	$V_{IN_SRC_ADC}$[4]	N/A	N/A	R	320mV.	
3	$V_{IN_SRC_ADC}$[3]	N/A	N/A	R	160mV.	
2	$V_{IN_SRC_ADC}$[2]	N/A	N/A	R	80mV.	
1	$V_{IN_SRC_ADC}$[1]	N/A	N/A	R	40mV.	
0	$V_{IN_SRC_ADC}$[0]	N/A	N/A	R	20mV.	

REG2Dh: ADC Result of the Output Current in Source Mode

Bit	Name	Default	Reset by WTD	R/W	Description	Comment
[15:8]	RESERVED	N/A	N/A	N/A	Reserved.	Reserved.
9	$I_{IN_SRC_ADC}$[9]	N/A	N/A	R	3200mA.	These bits indicate the result of the ADC conversion for the output current in source mode.
8	$I_{IN_SRC_ADC}$[8]	N/A	N/A	R	1600mA.	
7	$I_{IN_SRC_ADC}$[7]	N/A	N/A	R	800mA.	
6	$I_{IN_SRC_ADC}$[6]	N/A	N/A	R	400mA.	
5	$I_{IN_SRC_ADC}$[5]	N/A	N/A	R	200mA.	
4	$I_{IN_SRC_ADC}$[4]	N/A	N/A	R	100mA.	
3	$I_{IN_SRC_ADC}$[3]	N/A	N/A	R	50mA.	
2	$I_{IN_SRC_ADC}$[2]	N/A	N/A	R	25mA.	
1	$I_{IN_SRC_ADC}$[1]	N/A	N/A	R	12.5mA.	
0	$I_{IN_SRC_ADC}$[0]	N/A	N/A	R	6.25mA.	

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APPLICATION INFORMATION

Selecting the Input Capacitor

The input capacitor absorbs the maximum ripple current from the PWM converter. In buck mode, the input current is discontinuous. The input RMS ripple current (I_{CIN_RMS}) can be calculated with Equation (3):

$$I_{CIN_RMS} = I_{SYS} x \frac{\sqrt{V_{SYS} x (V_{IN} - V_{SYS})}}{V_{IN}} \quad (3)$$

The worst-case RMS ripple current occurs at 50% duty cycle. The SYS voltage (V_{SYS}) is about 8V while the battery is configured for 2 cells, so the worst-case condition occurs when input is between 15V and 20V.

Low-ESR ceramic capacitors with X7R or X5R dielectrics are recommended to be the input decoupling capacitor, and their voltage rating must exceed the normal input voltage level. For example, if there is a 20V input voltage, it is recommended to use a capacitor with a voltage rating that is at least 25V. These capacitors should be placed as close as possible to the IN and PGND pins. For input current limits up to 3A, it is recommended to use one 1μF capacitor and five 10μF capacitors.

VCC Decoupling Capacitor

VCC is an internal LDO output. An external 4.7μF decoupling capacitor must be placed between VCC and AGND, and as close as possible to these pins.

Selecting the Inductor

The MP2760 can operate in buck more or boost mode, so the inductor current is equal to either the charging current (I_{CHG}) or the input current (I_{IN}). The inductor saturation current should exceed the larger value between I_{IN} and I_{CHG}, plus half of the ripple current. The inductor current ripple for buck mode (I_{RIPPLE_BUCK}) and boost mode (I_{RIPPLE_BOOST}) can be calculated with Equation (4) and Equation (5), respectively:

$$I_{RIPPLE_BUCK} = \frac{V_{SYS} x (V_{IN} - V_{SYS})}{V_{IN} x f_{SW} x L} \quad (4)$$

$$I_{RIPPLE_BOOST} = \frac{V_{IN} x (V_{SYS} - V_{IN})}{V_{SYS} x f_{SW} x L} \quad (5)$$

The inductor ripple current (I_{RIPPLE}) depends on the input voltage (V_{IN}), the output system voltage (V_{SYS}), the switching frequency (f_{SW}) and the inductance (L).

The inductance (L) in buck mode can be calculated with Equation (6):

$$L = \frac{V_{SYS} x (V_{IN} - V_{SYS})}{I_{RIPPLE_BUCK} x V_{IN} x f_{SW}} \quad (6)$$

Table 5 lists how to select the inductance based on different voltages in buck mode.

Table 5: Inductor Values in Buck Mode

Specs	Inductance Selection			
V_{IN}	Conditions	L_{MIN}	L	I_{SAT}
9V	I_{SYS} = 6A, I_{RIPPLE_BUCK} = 50% x I_{SYS}, f_{SW} = 600kHz	0.5μH	1.5μH	>7.0A
12V		1.5μH	1.5μH	>9.0A
15V		2.1μH	2.5μH	>8.5A
20V		2.7μH	2.5μH	>9.2A

The required inductance (L) in boost mode can be estimated with Equation (7):

$$L = \frac{V_{IN} x (V_{SYS} - V_{IN})}{V_{SYS} x f_{SW} x I_{RIPPLE_BOOST}} \quad (7)$$

Table 6 lists how to select the inductance based on different voltages in boost mode.

Table 6: Inductor Values in Boost Mode

Specs	Inductance Selection			
V_{IN}	Conditions	L_{MIN}	L	I_{SAT}
5V	I_{SYS} = 6A, I_{RIPPLE_BOOST} = 50% x I_{SYS}, f_{SW} = 600kHz	1.1μH	1.5μH	>8A

If V_{SYS} is about 8V while the battery is configured for 2 cells, a 1.5μH inductor with a >7.5A saturation current is recommended for most specifications.

For applications that can support a higher ripple current, a lower-value inductor can be used to reduce PCB size.

Selecting the Output Capacitor

The output system capacitor (C_{SYS}) should have a ripple current rating that can absorb the output AC current, as well as sufficient

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capacitance to maintain the small output voltage ripple. In the boost mode, the output current is discontinuous and dominates the output RMS ripple current (I_{CSYS_BOOST}), which can be calculated with Equation (8)

$$I_{CSYS_BOOST} = I_{SYS} x \frac{\sqrt{V_{IN} \times (V_{SYS} - V_{IN})}}{V_{IN}} \quad (8)$$

The worst-case output RMS ripple current occurs at the lowest V_{BUS} input voltage. The SYS voltage is approximately 8V for the 2-cell battery configuration, so the worst case is the 5V source mode condition. Low-ESR ceramic capacitors, such as X7R or X5R, are preferred for the output decoupling capacitor, and should be placed close to the SYS and PGND pins of the IC.

The voltage rating of the capacitor must be exceed the normal battery voltage level. A capacitor with a 16V or greater voltage rating is recommended for 2-cell battery configurations. For a 6A charging current, it is recommended to use one 1μF capacitor and four 22μF capacitors.

Current Sense

The MP2760 has current loops to limit the current and improve the current accuracy and loop stability. An external current-sense resistor is required to sense the average current (see Figure 19).

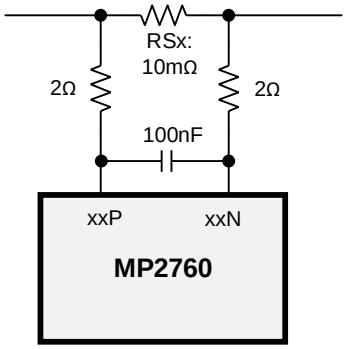

Figure 19: Input Current-Sensing Circuit

The input current loop limits the current drawn from the USB port. The input current is sensed through IAP and IAN.

The battery current loop limits the battery's charge current and discharge current. The battery current is sensed through SRP and SRN.

NTC Sense Resistor Divider

In real applications, an external negative temperature coefficient (NTC) thermistor is placed close to the battery to sense the battery's temperature. The MP2760 measures the battery temperature by monitoring the voltage ratio between the NTC and VNTC pins (see Figure 10 on page 32). Every temperature corresponds to a voltage ratio. The MP2760 has four temperature thresholds to satisfy JEITA requirements.

For a given NTC thermistor, the NTC hot and cold temperature points can be calculated with Equation (9) and Equation (10), respectively:

$$\frac{R_{T2} + R_{NTC_HOT}}{R_{T1} + R_{T2} + R_{NTC_HOT}} = \frac{V_{HOT}}{V_{VNTC}} \quad (9)$$

$$\frac{R_{T2} + R_{NTC_COLD}}{R_{T1} + R_{T2} + R_{NTC_COLD}} = \frac{V_{COLD}}{V_{VNTC}} \quad (10)$$

Where R_{NTC_HOT} is the thermistor value at the expected hot temperature protection point, and R_{NTC_COLD} is the thermistor value at the expected cold temperature protection point. V_{HOT} / V_{VNTC} and V_{COLD} / V_{VNTC} are 23.6% and 74.5%, respectively.

By default, V_{HOT} / V_{VNTC}, V_{WARM} / V_{VNTC}, V_{COOL} / V_{VNTC} and V_{COLD} / V_{VNTC} are 23.6%, 65.2%, 33.2%, and 74.5%, respectively.

Consider a 103AT NTC thermistor on the battery pack, where the thermistor parameters are $R_{25°C}$ = 10kΩ, β_factor = 3435K. If R_{T1} = 9.845kΩ and R_{T2} = 60Ω, the expected temperature thresholds (T_{HOT} = 60°C, T_{WARM} = 45°C, T_{COOL} = 10°C, and T_{COLD} = 0°C) can be determined.

For simplification, a 10kΩ R_{T1} can be used, and R_{T2} can be replaced with a wire.

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PCB Layout Guidelines

Efficient PCB layout is critical for specified noise, efficiency, and stability requirements. A 4-layer layout is recommended. For the best performance, refer to Figure 20 and follow the guidelines below:

1. Place the SYS output capacitors as close to SYS and PGND as possible. Place a small (such as 0603) 1μF capacitor closer to SYS and PGND than the 22μF capacitors. Ground connections must be tied to the IC ground with a short copper trace connection or PGND plane.
2. Place the input capacitors as close to IN and PGND as possible. Place a small (such as 0603) 1μF capacitor closer to IN and PGND than the other 10μF capacitors. Ground connections must be tied to the IC ground with a short copper trace connection or PGND plane.
3. The connection from SYS/IN to the 1μF must be routed on the same layer with the IC, the returning back to PGND also has to be on the same layer with the IC. Keep the whole routing loop as small as possible.
4. Connect AGND to PGND to each decoupling capacitor via a single-point connection.
5. Place the VCC decoupling capacitor and the bootstrap capacitors next to the IC and make trace connections as short as possible.
6. A Kelvin connection is required for the current-sense resistor.
7. Route current sense wires (IAP and IAN, SRP and SRN) away from switching nodes such as SW1 and SW2.

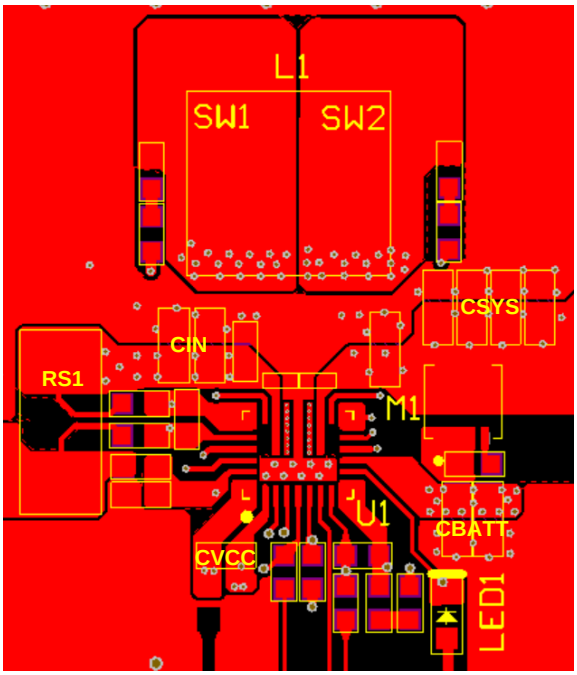

Figure 20: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

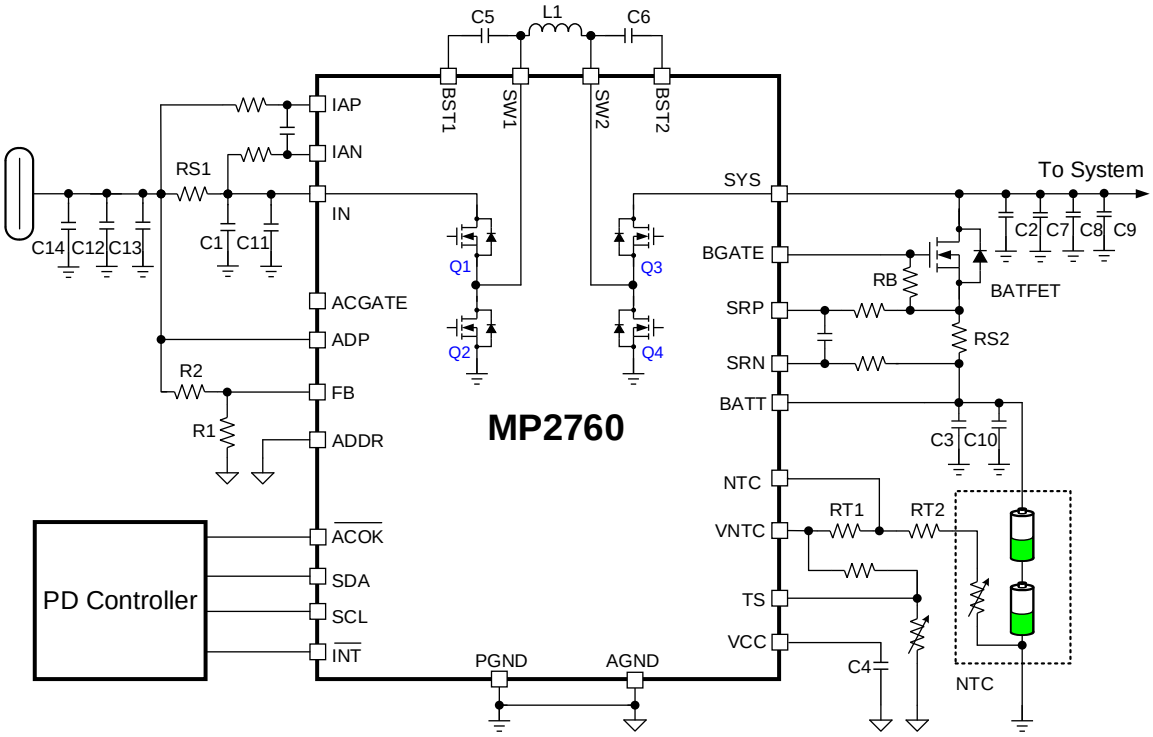

Figure 21: Typical Application Circuit

Table 7: Key BOM for Figure 21

Qty	Ref	Value	Description	Package	Manufacturer
5	C1, C11, C12, C13, C14	10µF	Ceramic capacitor, 25V, X7S	0805	Any
6	C2, C3, C7, C8, C9, C10	22µF	Ceramic capacitor, 25V, X5R or X7R	0805	Any
1	C4	4.7µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
2	C5, C6	100nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	L1	1.5µH	Inductor, 1.5µH, low DCR, I_{SAT} >14A	SMD	Any
2	RS1, RS2	10mΩ	Film resistor, 1%	2512	Any
1	BATFET	SISA14DN-T1-GE3	N-Channel MOSFET, 30V, 5.1mΩ; 20A	Power PAK 1212-8	Vishay
1	RB	5MΩ	Film resistor, 5%	0603	Any

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TYPICAL APPLICATION CIRCUITS *(continued)*

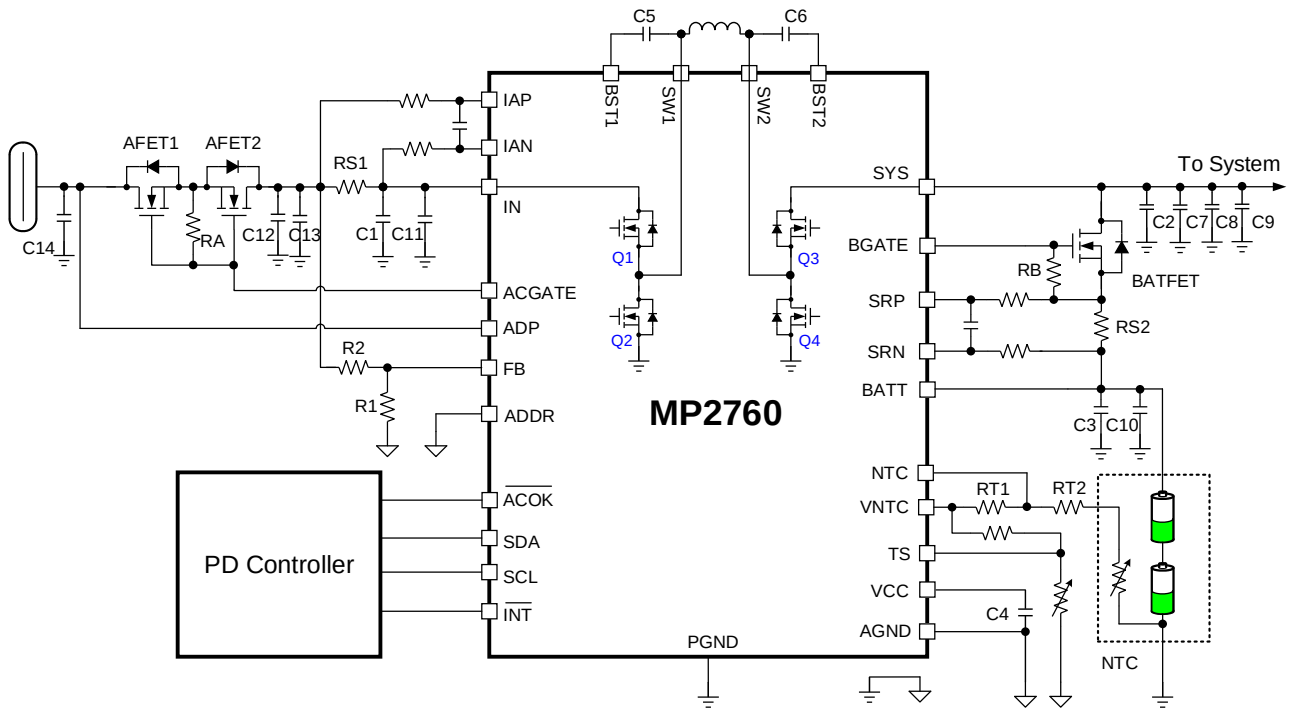

Figure 22: Typical Application Circuit with Input Disconnect Control

Table 8: Key BOM for Figure 22

Qty	Ref	Value	Description	Package	Manufacturer
5	C1, C11, C12, C13, C14	10µF	Ceramic capacitor, 25V, X7S	0805	Any
6	C2, C3, C7, C8, C9, C10	22µF	Ceramic capacitor, 25V, X5R or X7R	0805	Any
1	C4	4.7µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
2	C5, C6	100nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	L1	1.5µH	Inductor, 1.5µH, low DCR, I_{SAT} >14A	SMD	Any
2	RS1, RS2	10mΩ	Film resistor, 1%	2512	Any
2	RA, RB	5MΩ	Film resistor, 5%	0603	Any
3	AFET1, AFET2, BATFET	SISA14DN-T1-GE3	N-channel MOSFET, 30V, 5.1mΩ, 20A	Power PAK 1212-8	Vishay

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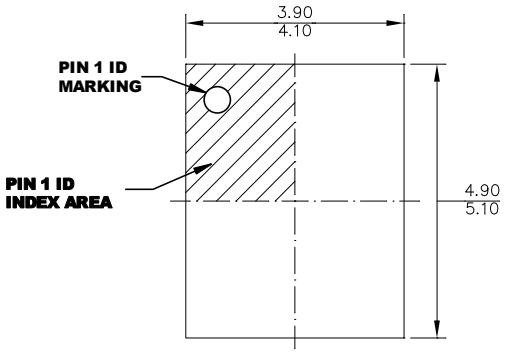
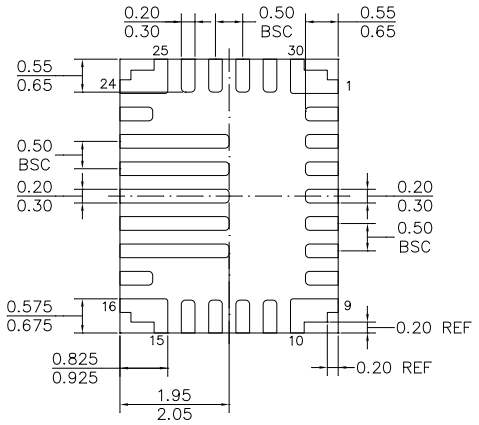
PACKAGE INFORMATION

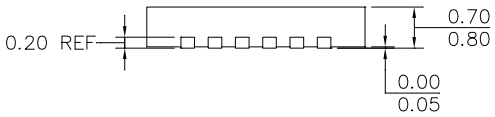
TQFN-30 (4mmx5mm)



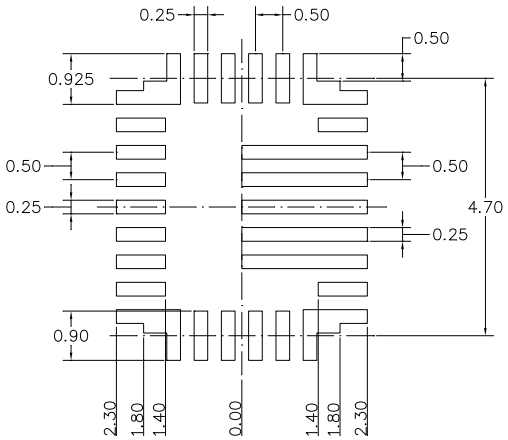
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

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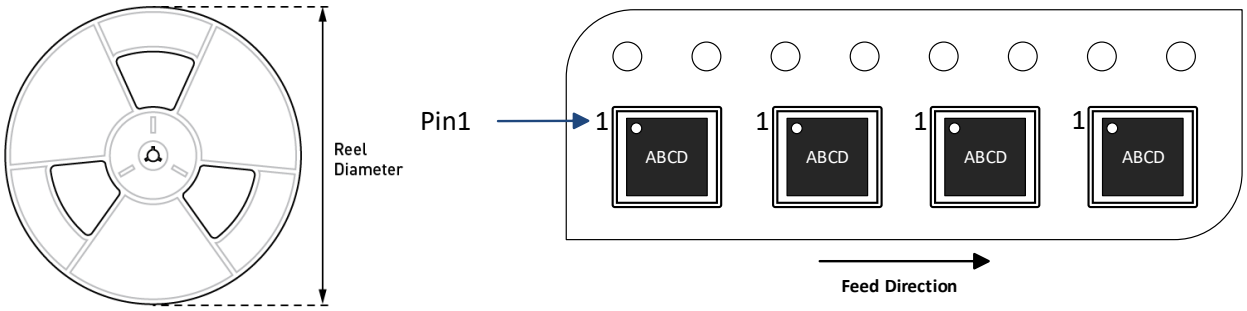
CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity /Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2760GVT-xxxx-Z	TQFN-30 (4mmx5mm)	5000	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/28/2021	Initial Release	-
1.1	8/8/2022	Updated the charged device model (CDM) to 750V	6
		Updated the electrical characteristics conditions (V_{BATT} = 3.7V/cell)	7–15
		Changed “Battery current in shipping mode” to “Battery standby current”	13
		Updated the test conditions for the battery quiescent current	14
		Updated the SMBus Timing Characteristics section and deleted the repeated items	15
		Change the axis-X of Efficiency vs. Charge current in charge mode (V_{BATT} = 4V) from “INPUT VOLTAGE (V)” to “CHARGE CURRENT (A)”	16
		Changed “OTG” to “SRC”	19–50
		Updated the REG06h, bit[7] name	39
		Updated the REG0Ah comments	41
		Updated the REG12h, bit[6] comment	49
		Changed REG16h, bits[15:14] = 00 to “Standby”	51
		Updated the REG16h and REG17h comments	51–53
		Updated table numbers	31–67
1.2	6/15/2023	Updated V_{OUT} in source mode to IN output voltage in source mode (V_{IN_SRC})	1, 6, 12, 34
		Updated I_{OUT} in source mode to IN output current in source mode (I_{IN_SRC})	1, 13, 34
		Updated the configurable output voltage from 3V to 21V to 4V to 21V	1, 26
		Added the default codes for 1-cell to 4-cell applications (MP2760GVT-010A, MP2760GVT-000A, MP2760GVT-030A, and MP2760GVT-040A, respectively), removed the note regarding the former “-0000” default code, and made formatting updates in the Ordering Information section	3
		Updated the descriptions of the VCC, ADDR, BST2, BST1, ACGATE, and FB pins in the Pin Functions section	5–6
		Updated the ADDR connection in Figure 2	25
		Added the HS-FET as well as a definition for the LS-FET to the Cycle-by-Cycle MOSFET Current Limit section	30
		Updated the condition for asserting an interrupt (INT) to “if the battery temperature is below V_{HOT} or above V_{COLD}” in the Battery Temperature Monitoring via the NTC Thermistor section; updated 0.1V/V and 0.1A/A to 0.1V/A in the IMON Function section	33
		Updated the quiescent current from 32µA to 33µA, and made a minor copyedit in the Battery Standby Mode section	34
		Updated the register reference from “REG18h~19h” to “REG18h and REG19h” in the Interrupt to Host (INT) section; updated the description (added references to the OTP address, REG05h, bits[6:3], and the universal address, 5Ch), updated Figure 14, and removed Table 5 in the Address section (previously Address Pin section)	35

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REVISION HISTORY *(continued)*

Revision #	Revision Date	Description	Pages Updated
		Moved Figure 16, Figure 17, and Figure 18	36
		Corrected the numbering of Note 6 and Note 7 (previously Note 7 and Note 8) and updated Note 6	37
		Added the default configuration for 2-cell applications (MP2760GVT-000A) to the section header; updated ADDR[3:0] (previously ADDR[6:3]), and reserved bit[7] and bits[2:0] in REG05h	38
		Updated the numbering of Table 5 and Table 6 (previously Table 6 and Table 7, respectively)	59
		Updated the V_{HOT} / V_{VNTC} value from 25% to 23.6%, and updated the 103AT thermistor example in the NTC Sense Resistor Divider section	60
		Removed R3 and updated the numbering of Table 7 (previously Table 8)	62
		Updated the numbering of Table 8 (previously Table 9)	63

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